DVCCTA based PID Controller with Grounded Passive Elements

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***Abstract* — This paper presents a Proportional Integral Derivative controller based on Differential Voltage Current Conveyor Transconductance Amplifier as an active element. In the proposed circuit, the PID parameters namely, Proportional gain constant, Integral time constant and Derivative time constant can be tuned electronically by varying the bias current of the circuit. All the passive elements used are grounded, making it suitable for on-chip implementation. This circuit can be utilized to realize PI and PD controller. The simulations are done in OrCAD PSPICE with 0.5µm CMOS MIETEC technology.**

Keywords—Differential Voltage Current Conveyor Transconductace Amplifier; PID controller; Voltage mode circuit.

I. INTRODUCTION

PID controllers are very important in signal processing systems. They are implemented in industrial and production plants to achieve steady state of unstable systems. PID controllers using op-amps are well described in the literature [1]. An op-amp based PID controller requires very large number of floating passive elements, which is undesirable for IC implementation. Furthermore, use of op-amp has limitations such as low bandwidth, large power consumption, and its operation also depends on the matching of used passive elements.

To overcome these limitations, a second generation current conveyor (CCII) based controller was designed in [2]. Despite of having many advantages over op-amp based controllers, they lack the ability to use floating or differential inputs. Differential Voltage Current Conveyor (DVCC) based controllers [3], overcome this disadvantage but lack electronic tuning capability, which is desirous in current signal processing industries. On the other hand Current Conveyor Transconductance Amplifier (CCTA) based controllers have tuning capability [4], but they lack the ability to use differential inputs.

Various PID controllers have been designed in literature using different techniques like OTA, DDCC, CCCCTA etc. but they all have limitations such as: use excess number of floating active or passive elements, does not have electronic tunability, PI and PD controller cannot be realized from the single circuit configuration, very complex circuitry [5 - 8].

A novel design of DVCCTA based PID controller is discussed in this paper. A Differential Voltage Current Conveyor Transconductance Amplifier (DVCCTA) is a current mode active building block which is a combination of DVCC and Transconductance Amplifier (TA). It possesses the characteristics of both DVCC and CCTA [9]. The PI and PD controllers can be realized from the same proposed circuit hence requiring a low chip area. It can also be tuned electronically without affecting the circuitry and is simple in design. Moreover all the passive elements used are grounded, making it suitable for IC implementation. The proposed circuit is simulated in OrCAD PSPICE with 0.5µm CMOS MIETEC technology.

The paper is arranged as follows: section II describes the DVCCTA block in brief. Section III proposes the DVCCTA based PID controller with relevant equations. Simulation results and conclusion are presented in section IV and V respectively.

II. DVCCTA

A DVCCTA is a current mode circuit which can work in current mode, voltage mode and mixed mode. This feature of DVCCTA makes it versatile and popular. There are other properties of DVCCTA which makes it attractive, such as: linearity, high bandwidth, high slew rate, wide dynamic range, electronically tunability, easy to use and implement [10].

DVCCTA has two voltage input terminals: Y1 and Y2, two current output terminals: O+ and O-, along with X and Z terminals [10]. The DVCCTA circuit symbol displaying current and voltages at these terminals is shown in Fig. 1. Fig.2. shows the equivalent circuit of the same.

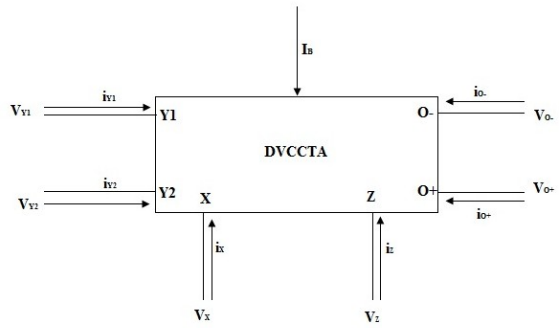

Fig. 1. DVCCTA circuit symbol

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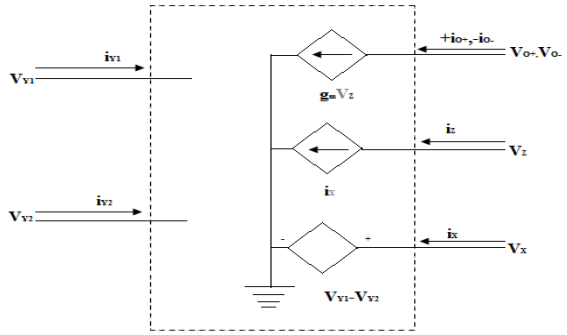


Fig. 2. DVCCTA equivalent circuit

The output-input relationship of ideal DVCCTA is[9]:

$$i_{Y1} = 0 \quad (1)$$

$$i_{Y2} = 0 \quad (2)$$

$$V_X = V_{Y1} - V_{Y2} \quad (3)$$

$$i_Z = i_X \quad (4)$$

$$i_{O\pm} = \pm g_m V_Z \quad (5)$$

and $$g_m = \sqrt{kI_B} \quad (6)$$

with constant, k as: $$k = \mu C_{ox} \frac{w}{l} \quad (7)$$

where, g_m - Transconductance gain, controlled by bias current I_B, μ - Mobility, C_{ox}- Gate oxide capacitance per unit area, w/l - Aspect Ratio.

III. Proposed Model

Fig. 3 shows the proposed PID controller based on DVCCTA. Here four DVCCTA blocks are used namely DVCCTA_BLOCK1, DVCCTA_BLOCK2, DVCCTA_BLOCK3 and DVCCTA_BLOCK4.

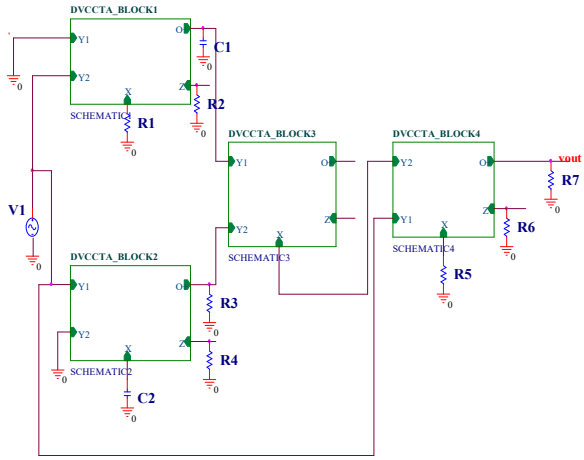


Fig. 3. Proposed PID controller.

A voltage source V1 is connected to the input terminals Y2, Y1 and Y1 of DVCCTA_BLOCK1, DVCCTA_BLOCK2 and DVCCTA_BLOCK4 respectively. All the passive elements are grounded.

$$V_{X1} = -V1 \quad (8)$$

$$i_{X1} = -\frac{V1}{R1} \quad (9)$$

V_{X1} and $V1$ are the voltage at X terminal and source voltage provided at DVCCTA_BLOCK, respectively. i_{X1} is the current at terminal X of DVCCTA_BLOCK1 and $R1$ is the resistance connected to it.

$$i_{X1} = i_{Z1} \quad (10)$$

According to the port relationship of DVCCTA, we know that the current at terminal X is passed to terminal Z. i_{Z1} is the current at terminal Z of DVCCTA_BLOCK1.

$$V_{Z1} = i_{Z1} \times R2 \quad (11)$$

V_{Z1} is the voltage at terminal Z and $R2$ is resistance connected to terminal Z.

$$i_{O1} = g_{m1} \times V_{Z1} \quad (12)$$

i_{O1} is the current at output terminal O and g_{m1} is the transconductance gain of DVCCTA_BLOCK1.

$$V_{O1}(s) = i_{O1} \times \frac{1}{sC1} \quad (13)$$

$V_{O1}(s)$ is voltage across terminal O and $C1$ is the capacitance connected to terminal O.

By using Eqns. (9)-(12) and putting it in Eqn. (13), we get:

$$V_{O1}(s) = -g_{m1} \times \frac{V1}{R1} \times R2 \times \frac{1}{sC1} \quad (14)$$

Similarly, we get the equations for DVCCTA_BLOCK2 as

$$V_{O2}(s) = g_{m2} \times V2 \times sC2 \times R4 \times R3 \quad (15)$$

where, $V_{O2}(s)$ is the voltage across terminal O, g_{m2} is the transconductance gain, $V2$ is the source given at terminal Y1, $C2$ is the capacitance at terminal X, $R4$ is the resistance at terminal Z and $R3$ is the resistance at terminal O of DVCCTA_BLOCK2.

$V_{O1}(s)$ and $V_{O2}(s)$ will be given as input to terminal Y1 and Y2 of D3 block.

$$V_{X3}(s) = V_{O1}(s) - V_{O2}(s) \quad (16)$$

$$V_{X3}(s) = -g_{m1} \times \frac{Vl(s)}{R1} \times R2 \times \frac{1}{sC_1} - g_{m2} \times V2(s) \times sC2 \times R4 \times R3 \quad (17)$$

$V_{X3}(s)$ is the voltage across terminal X of DVCCTA_BLOCK3, which will be provided as input to Y2 terminal of DVCCTA_BLOCK4.

Similarly, we get the equations for DVCCTA_BLOCK4.

$$V_{X4}(s) = V3(s) - V_{X3}(s) \quad (18)$$

$$V_{X4}(s) = V3(s) + g_{m1} \times \frac{Vl(s)}{R1} \times R2 \times \frac{1}{sC1} + g_{m2} \times V2(s) \times sC2 \times R4 \times R3 \quad (19)$$

$$i_{X4} = \frac{V3(s) + g_{m1} \times \frac{Vl(s)}{R1} \times R2 \times \frac{1}{sC1} + g_{m2} \times V2(s) \times sC2 \times R4 \times R3}{R5} \quad (20)$$

where, $V_{X4}(s)$, $V3(s)$, i_{X4} and $R5$ are the voltage at terminal X, input voltage at terminal Y1, current at terminal X and resistance at terminal X of DVCCTA_BLOCK4, respectively.

$$V_{out}(s) = V_{O4}(s) = g_{m4} \times \frac{V3(s) + g_{m1} \times \frac{Vl(s)}{R1} \times R2 \times \frac{1}{sC1} + g_{m2} \times V2(s) \times sC2 \times R4 \times R3}{R5} \times R6 \times R7 \quad (21)$$

$V_{out}(s)$, g_{m4}, $R6$, $R7$ are the voltage across terminal O, transconductance gain, resistance at terminal Z and resistance at terminal O of DVCCTA_BLOCK4 block, respectively.

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{gm_4 \times R6 \times R7}{R_5} \left(1 + \frac{1}{s\frac{C1 \times R1}{g_{m1} \times R2}} + sC2 \times R4 \times R3 \times g_{m2} \right) \quad (22)$$

The transfer function of PID controller is given in Eqn.23

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = K_p \left(1 + \frac{1}{sT_I} + sT_D \right) \quad (23)$$

Comparing, Eqns. (22) and (23), we get

$$K_P = \frac{g_{m4} \times R6 \times R7}{R_5} \quad (24)$$

$$T_I = \frac{C1 \times R1}{g_{m1} \times R2} \quad (25)$$

$$T_D = C2 \times R4 \times R3 \times g_{m2} \quad (26)$$

where, K_P, T_I and T_D is defined as proportional gain, integral time constant and derivative time constant, respectively. Circuit shown in Fig. 3 can be used to realize PI and PD controller. For PI controller ground the Y2 terminal of DVCCTA_BLOCK 3 and for PD controller attach a ground supply to Y1 terminal of DVCCTA_BLOCK 3.

We can tune the PID controller without affecting the passive elements by changing the bias current of DVCCTA_BLOCK4.

IV. Simulation Results

The basic building block DVCCTA is designed using 0.5µm CMOS MIETEC model in ORCAD Pspice. The internal CMOS structure of DVCCTA and the aspect ratios has been referred from [10]. The DC bias voltages used are V± = 1.5V and VB = -0.77V. IB is fixed for all the blocks at 100µA. As mentioned earlier, the PID parameters can be varied by varying this bias current IB, keeping the other circuit parameters unchanged. Table I lists the value of parameters used in our simulation.

TABLE I. CIRCUIT PARAMETERS

DVCCTA_BLOCK1	R1=10k, R2=5k, C1=50p
DVCCTA_BLOCK2	R3=10k, R4=5k, C2=50p
DVCCTA_BLOCK4	R5=10k, R6=5k, R3=20k

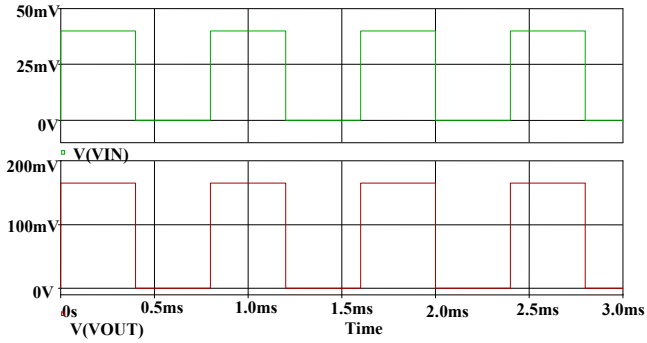


Fig. 4. Open loop response of Proportional Block of proposed PID Controller

Fig. 4. shows the time domain response for the Proportional block, i.e. DVCCTA_BLOCK4 of Fig. 3. We have performed simulations using step input, the responses show that the output of system is in phase and amplified. Hence, verifying the performance of designed circuit.

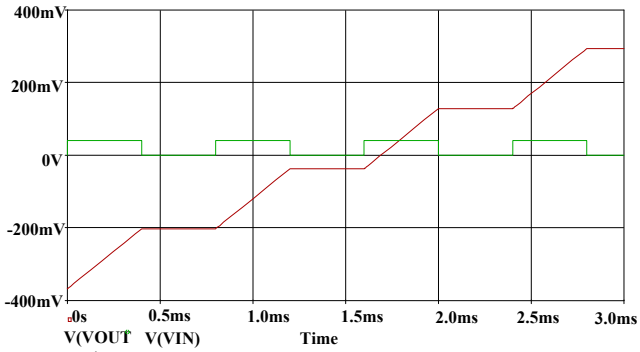


Fig.5. Open loop response of Integral block of proposed PID Controller

Block 1 in Fig. 3 is the Integral block. From Fig. 5, it can be seen that a step input provides the ramp output; which is in compliance with the theoretical concept of integration.

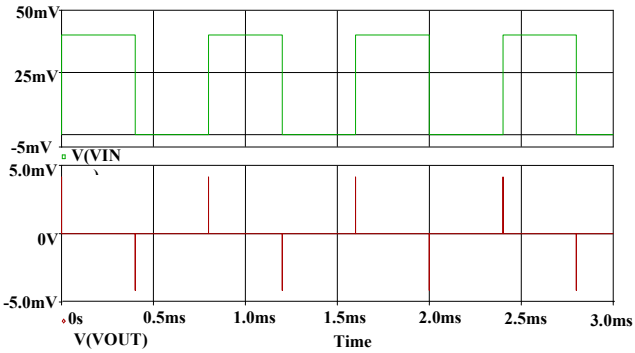


Fig. 6. Open loop response of Derivative block of proposed PID Controller

DVCCTA_Block 2 of Fig. 3 is the Derivative block and from the time domain response of Fig. 6, it is observed that the derivative block is generating appropriate output for the provided input signal, i.e. impulse response is attained for a step input.

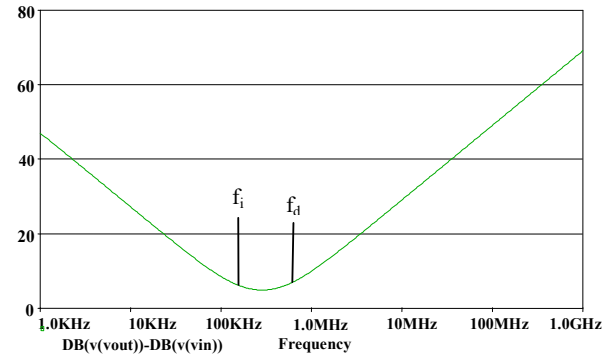


Fig. 7. Gain vs. Frequency curve of proposed PID controller

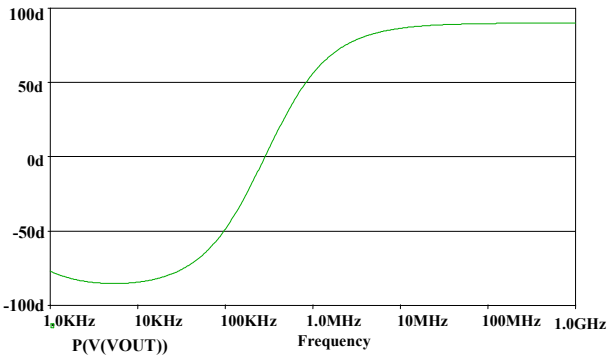


Fig. 8. Phase response of proposed PID controller

Figues 7 and 8 show the simulated gain and phase responses of the proposed PID controller (Fig. 3), respectively. The schematic is simulated with 40mV AC input. It is observed that the integral frequency (fi) is 167 KHz and derivative frequency (f_d) is 588 KHz.

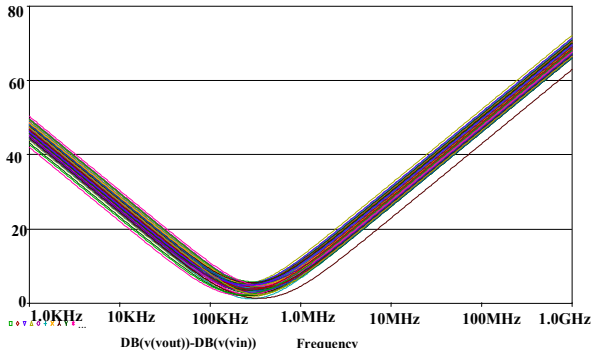


Fig. 9. Monte-Carlo simulation for all resistances with 10% tolerance of PID controller

Monte-Carlo analysis of the gain using 10% Gaussian tolerances for all resistances using 50 runs, is shown in Fig. 9. These results confirm the stability and robustness of the circuit in frequency domain.

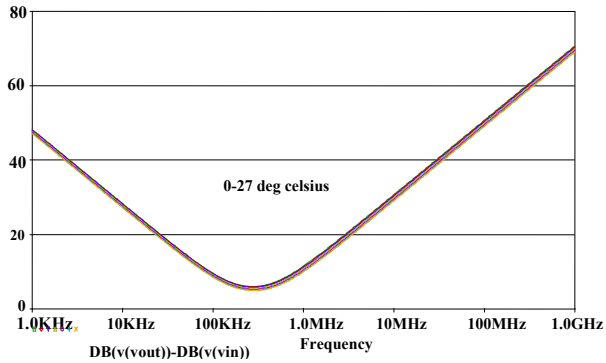


Fig. 10. Simulated gain response when temperature is varied.

The simulated gain response of PID controller when temperature is varied from 0^O C to 27^O C is shown in Fig 10. It is concluded from the same, that the system shows stability in this temperature range.

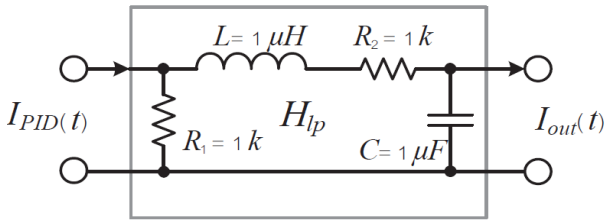


Fig. 11. LPF Circuit used as plant for the closed loop system.

The passive elements of the filter in Fig. 11 were determined by R1=R2=1k, L=1µH and C=1µF. Fig. 12 shows frequency response of passive low-pass filter, which works as the plant for closed loop control system.

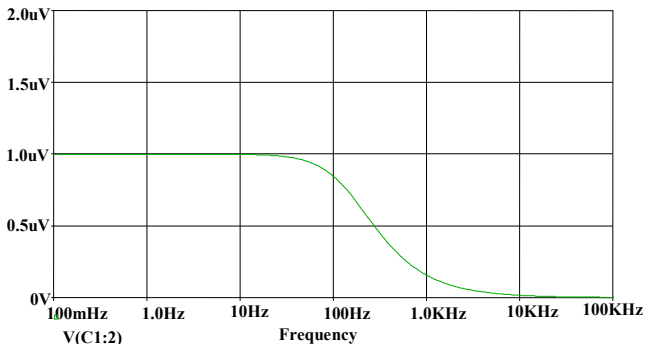


Fig. 12. Open loop response of Low Pass Filter

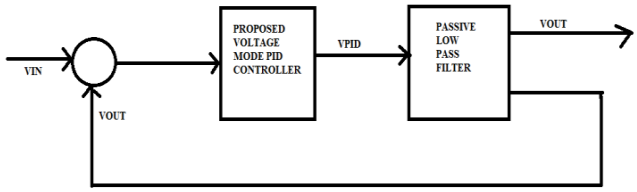
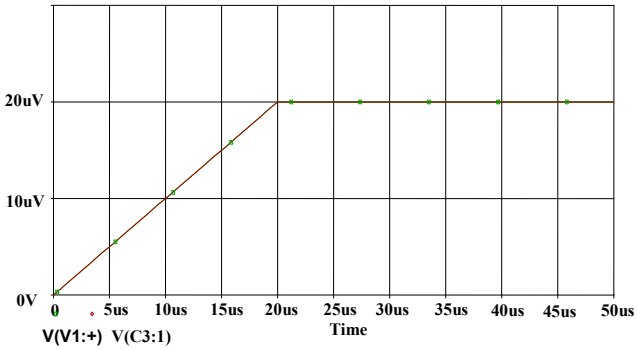
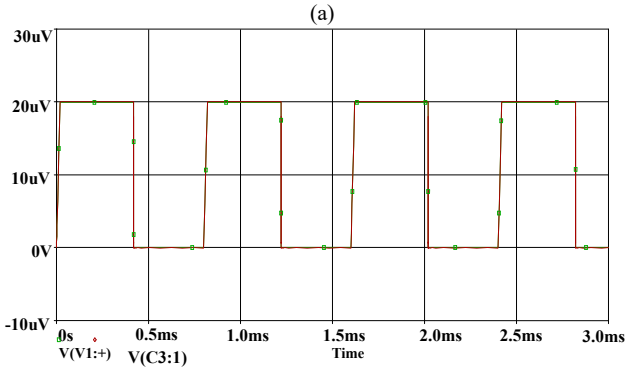


Fig. 13. Closed loop System with proposed PID controller and LPF as plant.

A unit step input is applied at the input of the closed loop system of Fig.13. The simulation results are presented in Fig. 14.



(a)



(b)

Fig. 14. Input Output relationship of closed loop control system

The response for closed loop control system (Fig. 13) is determined, with an input step signal (VIN) of peak value 20µA at 1 kHz frequency. Fig. 14 (a) shows the transient response of one of three periods when comparing input signal to output signal of a closed loop control system of circuit shown in Fig. 13. where bias current for all the DVCCTA blocks used in proposed PID controller is 100µA. Fig.14 (b) illustrates the input output relationship in steady state situation. From these results, we observed that the error is minimized and system is controlled or stabilized.

V. Conclusion

In this paper, a DVCCTA based voltage mode PID controller is presented. The proposed model employs four DVCCTA blocks with all passive elements grounded. The circuit is very convenient for IC implementation. The PI, PD and PID controller can be realized by the same proposed circuit by appropriately selecting the input terminals. This proposed design is more dynamic than the previous techniques used to make PID controllers and provides wider bandwidth, higher dynamic range and has electronic tuning capability. It can tune the gain of the system without affecting the circuitry.

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