# Low Power Adiabatic 4-Bit Johnson Counter based on Power-Gating CPAL Logic

Garima Bhargave
Dept. of Electronics and Communication Engineering, IGDTUW,
Kashmere Gate, Delhi-110006, India
g.bhargav33@gmail.com

Priyanka Sheokand
Dept. of Electronics and Communication Engineering, IGDTUW,
Kashmere Gate, Delhi-110006, India

Sarita Uniyal
Dept. of Electronics and Communication Engineering, IGDTUW,
Kashmere Gate, Delhi-110006, India

***Abstract*—This In this paper, a different power saving adiabatic 4- bit Johnson counter based on two-phase CPAL circuits with power gating method is proposed. The power dissipation of proposed adiabatic Johnson counter comes out to be 16.3µW, 10µW, 9.2µW, 5.6µW and 10.9µW for frequencies 5MHz, 10MHz, 20 MHz ,50 MHz and 100MHz respectively with a load capacitance of 10fF. Proposed design saves more power in comparison to CMOS logic in frequency range of 5MHz to 100MHz. Further, the basic gates using two phase CPAL circuits have been designed and simulated. The designed circuits are simulated in Tanner ECAD tool with 90nm technology.**

***Keywords—Two-phase CPAL, power gating, Johnson counter, TANNER ECAD.***

## I. INTRODUCTION

Low power circuit design has come into view as one of the important matter of concern in VLSI design because of the development of portable devices. As the feature size is shrinking gradually , leakage power dissipation is becoming a major constituent of the power dissipation[1] in deep submicron circuits. Thus, power dissipation in standby mode has become an important factor thus attracting extensive applications [2-4].

Adiabatic logic is an effective technique which reduces the power dissipation. It recycles a part of output energy back to the source, thus lowering the amount of power dissipated as heat. Many families based on adiabatic logic such as ECRL, PFAL, 2 PASCL, CPAL etc have been reported. Considerable amount of energy savings have been achieved by these logics[5,6,7,8]. It is well known that in CMOS (static) circuits , there is no switching power dissipation for constant input signals. Although, in adiabatic circuits, the energy dissipation occurs even for input signals which are constant[9]. Again, with the CMOS technology continuously being scaled, leakage power dissipation in adiabatic circuits has become a matter of serious concern. To minimize this power dissipation, several power gating methods have been brought into consideration [10,11]. For sequential circuits, low power design is considered to be very powerful for good performance of any digital circuitry. For different types of logic, different kinds of counters are invented. Johnson counter is an extremely useful counter system because it provides the required kind of data synchronously in a loop in a sequential manner. This counter can be used in various logic designs and applications.

In this paper ,a power saving design scheme of 4-bit Johnson counter using Complementary pass transistor adiabatic logic (CPAL) using power gating scheme is presented.

This paper is segmented into five parts. Part II describes the two phase CPAL gates. Part III describes the power gating scheme for CPAL circuits. Part IV describes the proposed design of Johnson counter. Part V concludes the paper.

## II. TWO PHASE CPAL GATES

### *A. Two phase CPAL buffer*

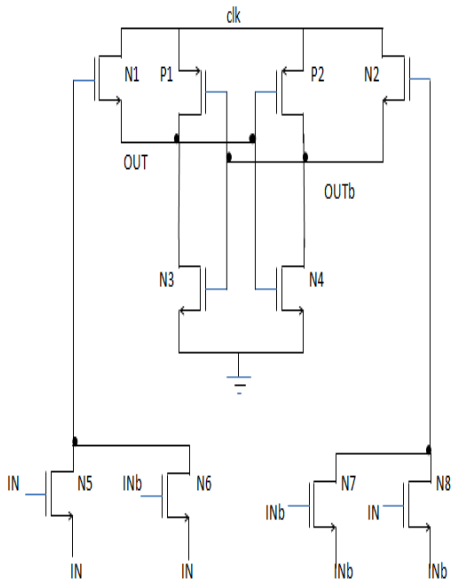


Fig. 1. Circuit implementation of two phase CPAL buffer

The basic structure of two phase CPAL buffer is shown in figure 1 [9] [12]. This structure mainly consists of two parts: one is circuit of logic function and the other is a load drive circuit. The logic function block has N5, N6, N7 and N8 transistors having CPL function block. The load drive circuit

978-1-4673-9080-4/16/$31.00 ©2016 IEEE

comprises transmission gates N1,P1 and N2,P2. The simulation results for the above circuit are shown in figure 2.

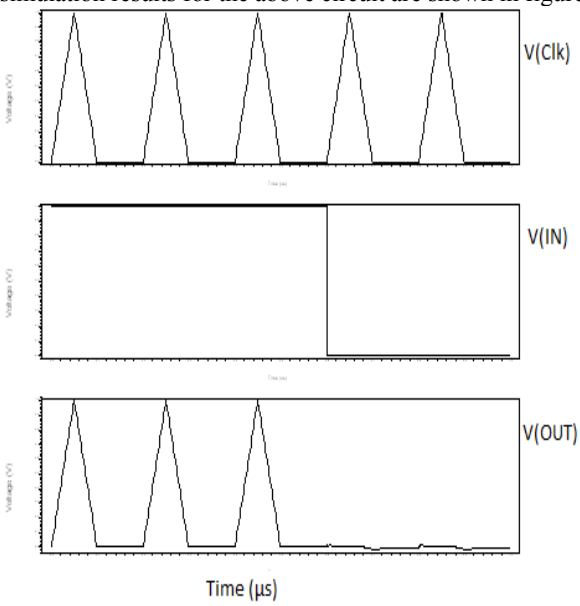


Fig. 2. Simulated Waveform for two phase CPAL buffer using a pulse source of 1V.

## B. *Two phase CPAL AND gate*

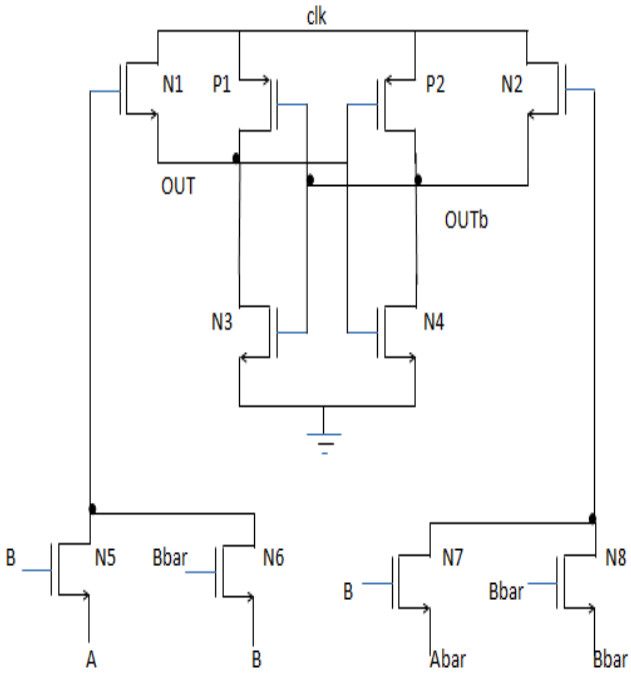


Fig.3. Circuit implementation for CPAL AND gate

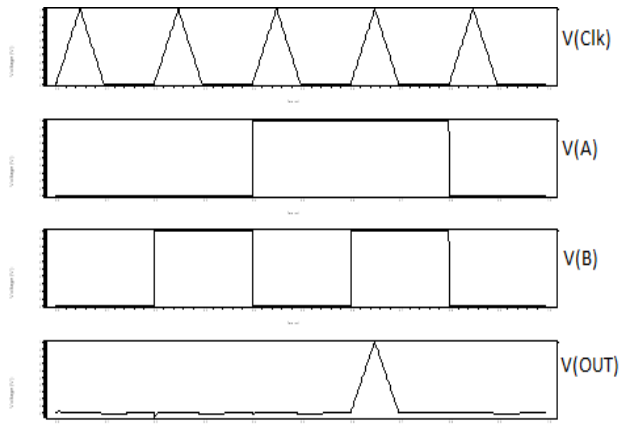


Fig. 4. Simulated Waveform for CPAL AND gate with a pulse source of 1 V.

## C. *Two phase CPAL OR gate*

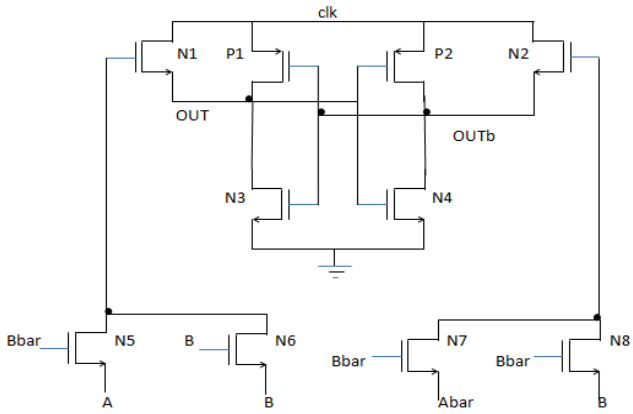


Fig. 5. Circuit diagram for OR gate

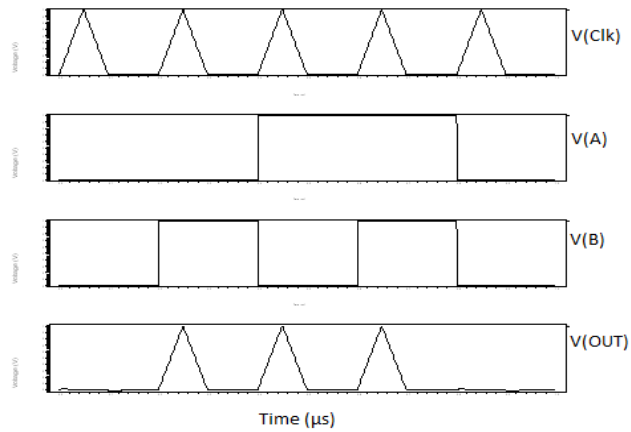


Fig. 6. Simulated Waveform for two phase CPAL OR gate with a pulse source of 1 V.

### D. *Two phase CPAL XOR gate*

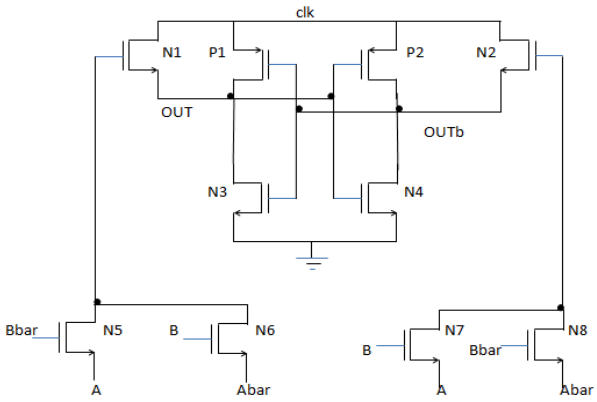


Fig. 7. Circuit implementation for CPAL XOR gate

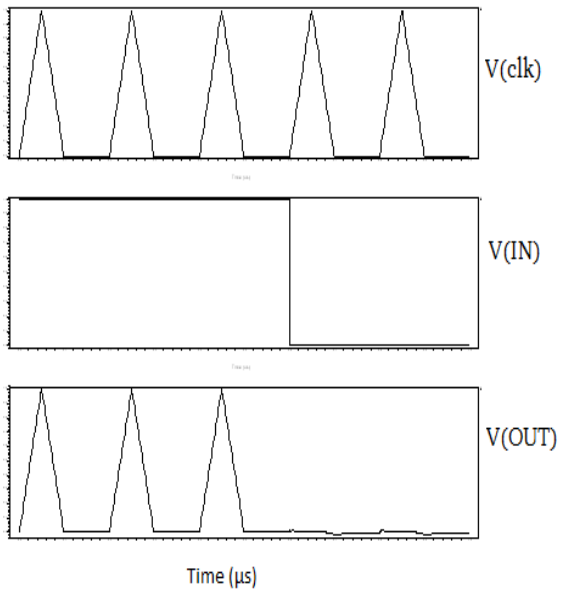


Figure 8: Simulated Waveform for CPAL XOR gate with a pulse source of 1V.

## III. POWER GATING SCHEME FOR CPAL CIRCUITS

To minimize energy losses in adiabatic units, this scheme is used[10,13]. For two phase adiabatic logic, two-phase power supplies, which are non- overlapping are used. Power gating switch as well as the power gating scheme using 2 phased CPAL is shown in figure 9: (a) and (b). Two power gating switches are used in this circuit. These power gating switches are realized by a CPAL using buffer chain. During sleep mode, these switches are used to cut the link between adiabatic logic and power clocks (Clk1 and Clk2) to minimize the losses. In the switches used for power gating, the transistors named N9 and N10 are used to make the nodes Z and Zb, which are un-driven, grounded. It is because the node Z or Zb will be lightly bootstrapped for even low level of PC or PCb. This being due to the large size of NMOS transistors N1 and N2.

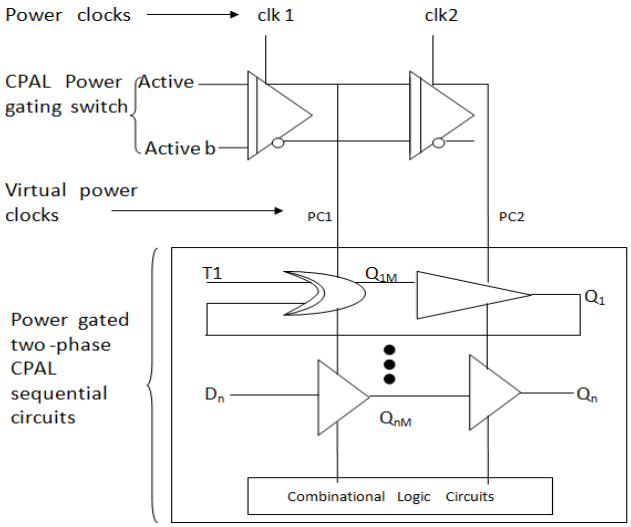


Fig. 9 (a) : Power gating scheme for 2 Phase CPAL

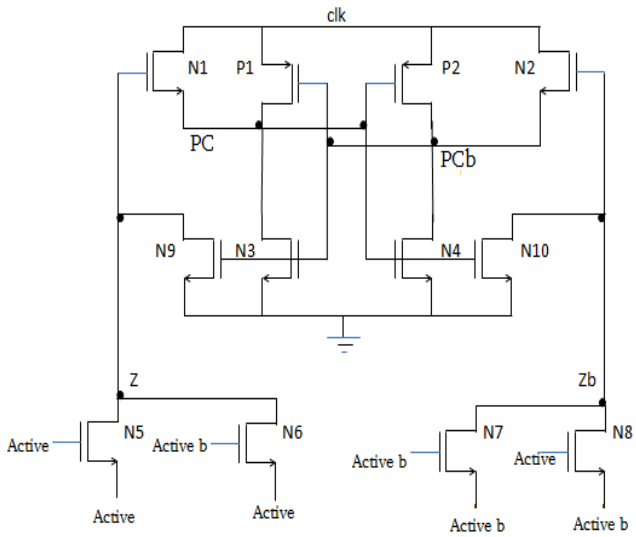


Fig. 9 (b): CPAL power gating switch

The simulation waveforms for the CPAL circuits are represented in figure 10. There are two modes of operation for the power- gated adiabatic circuits under control of *ENABLE (*active) signal. Virtual clock signals (PC1 and PC2) follow power clocks (Clk1 and Clk2) as signal active is high in active mode. This will ensure proper operation of the required

logic(adiabatic) block. Hence, the scope of power losses during sleep mode is minimized.

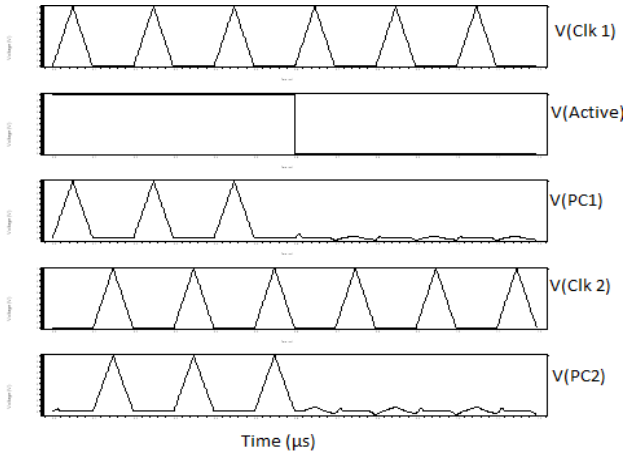


Fig. 10: Simulated Waveform for virtual power clock signals

## IV. 4-BIT ADIABATIC JOHNSON COUNTER POWER GATING SCHEME

Various previous adiabatic logic styles centered mainly on combinational logic designs. In this section, design and analysis of an adiabatic sequential circuit is presented [8,14]. A new Johnson counter scheme is represented in figure 11. The proposed 4-bit Johnson counter consists of four D flip flops which are implemented using a two phase CPAL buffer chain. Each flip flop gets a virtual power clock when it is required to replicate the value saved in it. The Johnson counter's output is exhibited in the truth table in TABLE 1.

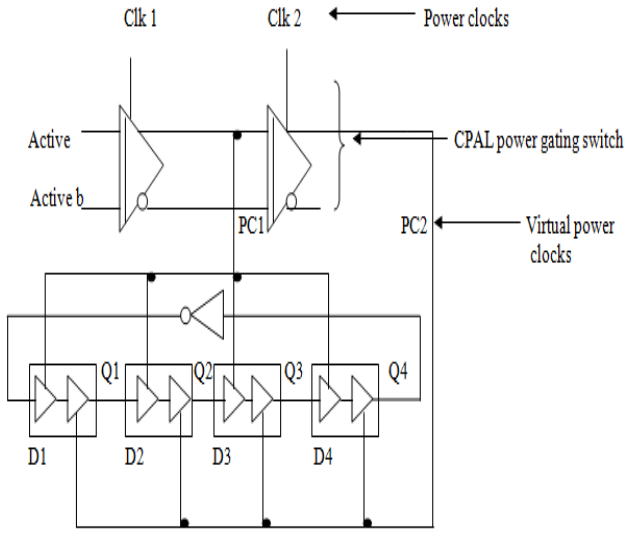


Fig. 11 : 4- bit adiabatic Johnson counter using CPAL with power gating scheme.

TABLE I. TRUTH TABLE FOR A 4- BIT JOHNSON COUNTER

| CLOCK | Q4 | Q3 | Q2 | Q1 |
|---|---|---|---|---|
| 1 | 0 | **0** | **0** | **0** |
| 2 | 1 | 0 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 |
| 4 | 1 | 1 | 1 | 0 |
| 5 | 1 | 1 | 1 | 1 |
| 6 | 0 | 1 | 1 | 1 |
| 7 | 0 | 0 | 1 | 1 |
| 8 | 0 | 0 | 0 | 1 |

The circuit has been simulated in TANNER ECAD tool using schematic simulation technique and the results are shown in figure 12.

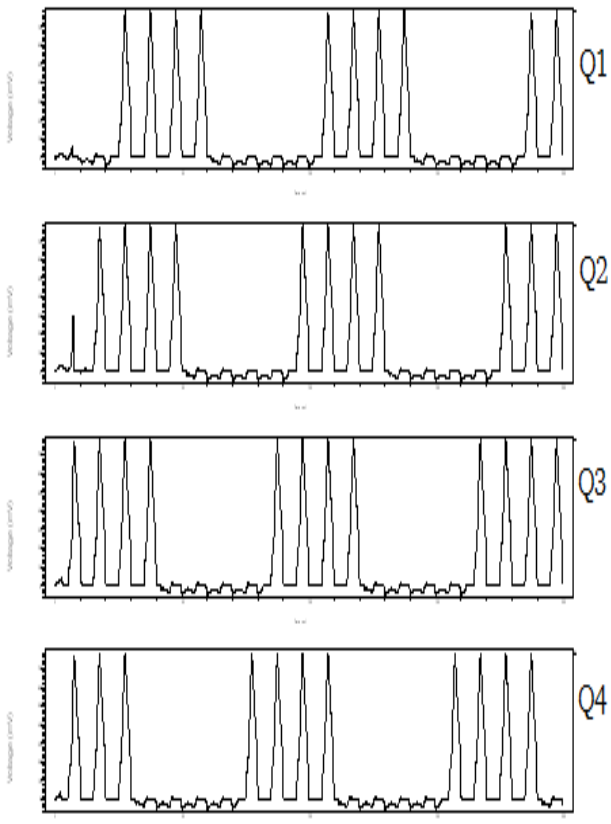


Figure 12: Simulated waveform for proposed Johnson counter

The counter is simulated using supply voltages in the range of 0.7V to 1.1V with a step voltage of 0.1V. Simulation results are shown in Figure 13. Also figure 14 shows the power dissipation comparison of the proposed 4- bit adiabatic Johnson counter with the conventional CMOS based Johnson counter for different frequencies at a source voltage of 0.8V.

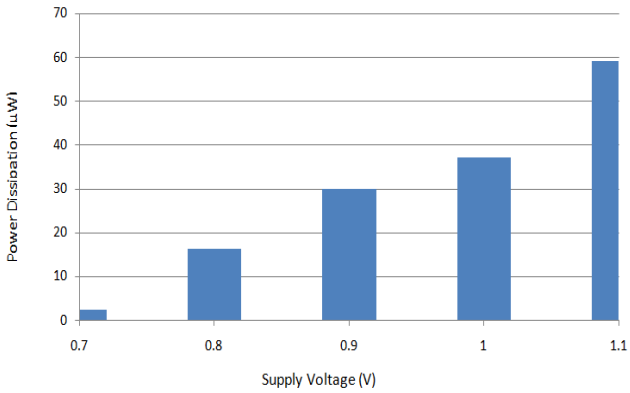


Fig.13. Power dissipation with respect to supply voltage at a frequency of 5MHz and load capacitance of 10fF.

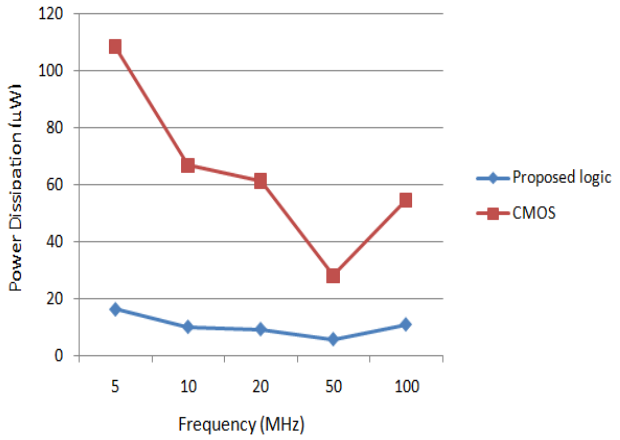


Fig.14. Power savings of adiabatic 4- bit Johnson counter using CPAL with power gating scheme compared with the conventional CMOS based design for different frequencies at a source voltage of 0.8V

## V. CONCLUSION

Design of Johnson counter and basic gates using Two phase CPAL circuits with power gating scheme is presented. Based on the simulation results, the proposed design dissipates only 10 to 15% power as compared to conventional CMOS logic in the frequency range of 5-100MHz. Hence, the logic comes out to be very promising and power efficient for low power VLSI applications.

## References


[1] Fallah, F. and Pedram, M. (2005), "Standby and Active Leakage Current Control and Minimization in CMOS VLSI Circuits", *IEICE Transactions on Electronics,* Vol. E88-C(4), pp. 509–519.

[2] Kim, N.S., Austin, T. *et al*. (2003), "Leakage Current: Moore's Law Meets Static Power", *Computer,* Vol. 36(12), pp. 68–75.

[3] Fallah, F. and Pedram, M. (2005), "Standby and Active Leakage Current Control and Minimization in CMOS VLSI Circuits", *IEICE Transactions on Electronics*, Vol. E88–C(4), pp. 509–519.

[4] Abdullah, A., Fallah, F. and Pedram, M. (2004), "Leakage Current Reduction in CMOS VLSI Circuits by Input Vector Control", *IEEE Trans. Very Large Scale Integration (VLSI),* Vol. 12(2), pp. 140–154.

[5] Moon, Y. and Jeong, D.K. (1996), "An Efficient Charge Recovery Logic Circuit", *IEEE J. of Solid-State Circuits*, Vol. 31(4), pp. 514–522.

[6] Hu, Jianping, Xu, Tiefeng, Yu, Junjun and Xia, Yinshui (2004), "Low Power Dual Transmission Gate Adiabatic Logic Circuits and Design of SRAM", in *Proc. IEEE MWSCAS'04*, pp. 565–568, Japan, 2004.

[7] Ng, K.W. and Lau, K.T. (2000), "Low Power Flip-flop Design based on PAL-2N Structure", *Microelectronics J*., Vol. 31(2), pp. 113–116.

[8] Hu, J.P., Xu, T.F. and Xia, Y.S. (2005), "Low-power Adiabatic Sequential Circuits with Complementary Pass-transistor Logic", *IEEE MWSCAS'05,* pp. 1398–1401, USA, August 7-10, 2005.

[9] Hu, Jianping, Xu, Tiefeng and Li, Hong (2005), "A Lower-power Register File based on Complementary Pass-transistor Adiabatic Logic", *IEICE Trans. on Inf. & Sys.,* Vol. E88–D (7), pp. 1479–1485.

[10] Zhou, D., Hu, J.P. and Wang, L. (2007), "Adiabatic Flip-flops for Power-down Applications", *IEEE ISIC,* pp. 493–496.

[11] Teichmann, P., Fischer, J. and Henzler, S. *et al.* (2005), "Power-clock Gating in Adiabatic Logic Circuits", in *Proc. PATMOS'05,* pp. 638–646.

[12] Zhou, Dong, Hu, Jianping and Dong, Huiying (2007), "An Energy-efficient Power-gating Adiabatic Circuits using Transmission Gate Switches", *IEEE ASICON'07*, pp. 145–148.

[13] Hu, Jianping, Zhou, Dong and Wang, Ling (2007), "Power-gating Adiabatic Flipflops and Sequential Logic Circuits", *IEEE ICCCAS'07*, Fukuoka, Japan, July 2007.

[14] Lin, Jianhui, Hu, Jianping and Chen, Qi (2011), "Low Voltage Adiabatic Flip-flops based on Power-gating CPAL Circuits", *Procedia Engineering*, Vol. 15 , pp. 3144–3148.