Performance Evaluation of SRAM Cells for Deep Submicron Technologies

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***Abstract*—In this paper, different Static RAM (SRAM) cell structures have been analysed in deep submicron regions. A 6T, 7T, 8T and 9T SRAM cell have been compared on the basis of Static Voltage Noise Margin (SVNM), Write Trip Voltage (WTV), Static Current Noise Margin (SINM), Write Trip Current (WTI), Active Leakage Current, Cell Standby Leakage Current, Read Current and Data Retention Voltage (DRV). The recent N-curve method is used over the traditionally used Butterfly Curve method for better analysis in submicron regions. The SRAM cell simulations are performed on 22nm, 32nm and 45nm CMOS technology nodes. The results show that the 6T SRAM cell has the poorest read and write margins and the highest active leakage, standby leakage and read currents across all technology nodes. Also, the 7T cell structure shows the best performance, exhibiting the highest write margins, the lowest active leakage current, lowest data retention voltage and the lowest read and standby-leakage currents across all technology nodes.**

Keywords—6T SRAM cell; 7T SRAM cell; N-Curve; Active Leakage Current; Static Voltage Noise Margin; Static Current Noise Margin; Write Trip Voltage; Write Trip Current; Standby Leakage Current; Read current; Data Retention Voltage.

I. INTRODUCTION

There is an ever growing need for low power portable devices. All portable devices have a high performance dedicated memory on the processor die itself called 'cache' [1]. This high performance memory is called the Static RAM (SRAM) [1], [2]. When designing or scaling a SRAM cell in submicron regions, one is faced with design challenges such as improving noise margins, reducing leakage power etc. [1]. Various cell designs have been proposed to combat the tradeoff between its read and write capability and improve its robustness, density and performance.

In this paper, the SRAM cell architectures using six transistors (6T), seven transistors (7T), eight transistors (8T) and nine transistors (9T) have been analysed in submicron regions. These structures have been simulated on the 22nm, 32nm and 45nm CMOS technology nodes [3] and their performance has been compared on the basis of Static Voltage Noise Margin (SVNM), Write Trip Voltage (WTV), Static Current Noise Margin (SINM), Write Trip Current (WTI), Active Leakage Current, Cell Standby Leakage Current, Read current and Data Retention Voltage (DRV). This paper describes the SRAM cell architectures in Section II. Thereafter in Section III, it explains the performance parameters of the cell, taking into consideration, the submicron region operating conditions. The simulation results of different cell structures and performance analysis is included in section IV. Finally, the section V concludes the paper.

II. CELL ARCHITECTURE

A. *The 6T SRAM Cell* [2]

The 6T SRAM cell comprises of two cross-coupled CMOS inverters (PUL-PDL, PUR-PDR) and two access transistors (ACL, ACR) for read and write operations [2]. A schematic of the 6T SRAM cell is shown in Fig. 1. The Word Line (WL) is enabled whenever the cell performs read/write operations and disabled during standby. During write operation, the data is put on the Bit Line (BL). The current flows from power supply to a data line through the PUL/PUR and ACL/ACR transistor pair to write the value into the cell. During read operation, both lines are clamped to V_{DD} using the pre-charge circuit. The bit line adjacent to the node storing zero is pulled down through the PDL or PDR transistor. This voltage drop is sensed by the sense amplifier which further converts it into low and high levels for usage by the external circuits. The cell preserves one of its two possible states, as long as the power supply is active. Since in the 6T cell, the read and write port is the same and optimization is made possible only through transistor sizing, the performance parameters aren't sufficiently desirable [2].

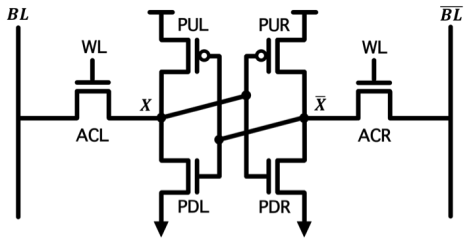

Fig. 1 : The 6T SRAM Cell [2]

B. *The 7T SRAM Cell* [4]

In this cell, the read and write ports are isolated as shown in Fig. 2 [4]. The cell has two cross coupled inverters along with a single access transistor (AC) used for writing into the cell [4]. The read port (RBL) has two NMOS transistor R1 and R2 for the purpose. Since the read operation has been separated in 7T, optimizing the transistor size for read operation isn't necessary. Thus, the pull down transistors can be made minimum feature size. During write operation, the value needed to be written is put on the BL. The word line is enabled and the value is

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overwritten into the cell. During read operation, the value stored in $\overline{X}$ node enables or disables R1. During read '1', R1 remains switched off and the read bit line remains at high level. During read '0', the R1 is switched on and the read bit line is pulled down through R2 and R1.

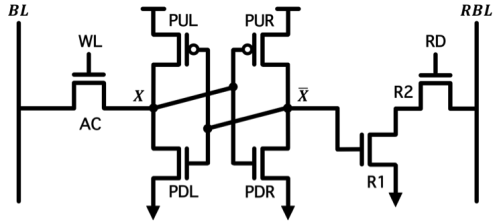


Fig 2 : The 7T SRAM Cell [4]

C. *The 8T SRAM Cell* [5]

The 8T SRAM cell also has isolated read and write port. In contrast to 7T, it has two access transistors (ACL, ACR) for write operation [5]. The read port remains isolated, therefore the pull down transistors can be made minimum feature size. During write operation, WL is pulled high and the value to be written is put on the BL. During the read operation, the value stored in $\overline{X}$ node enables or disables R1. During read '1', R1 remains switched off and the read bit line remains at high level. During read '0', the R1 is switched on and the read bit line is pulled down through R2 and R1.

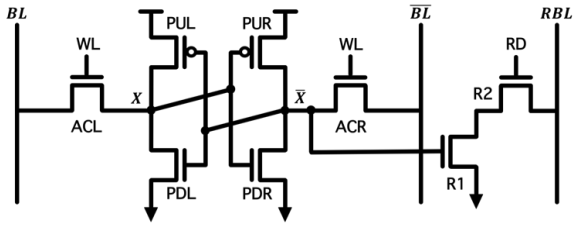


Fig. 3 : The 8T SRAM Cell [5]

D. *The 9T SRAM Cell* [6]

The 9T isolates its reading port but unlike 7T or 8T, uses the same set of bit lines to both read and write [6]. During write operation, the word line is pulled high and the data is put on the BL. During read operation, the R1 transistor is turned on and word lines are kept low. Either of the RL and RR transistors are turned on according to the value stored in cell. Consequently, the BL or $\overline{BL}$ is pulled down through RL/RR and R1.

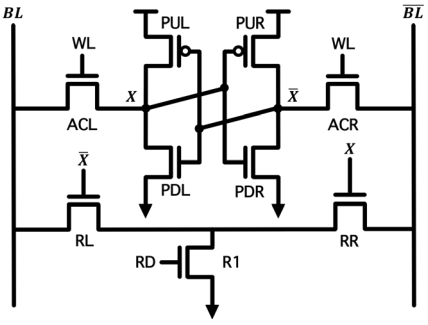


Fig. 4 : The 9T SRAM Cell [6]

III. Performance Parameters

A. *Noise Margins*

Noise Margins indicate stability in SRAM cells. Measuring noise margins is necessary to ascertain that inadvertent destruction of data stored in the cells doesn't take place. The Static Noise Margin using the Butterfly Curve plots the X and $\overline{X}$ node voltages as one is swept from zero to V_{DD} [7]. The traditional Static Noise Margin using butterfly curve has its disadvantages in submicron technologies. After measuring the Butterfly curve, further mathematical analysis is required to be done for calculating final noise margin values [8]. Another disadvantage is that it doesn't give any information about the current usage of the SRAM cell or explain about cells with same noise margin and different performance [8]. An alternate definition of SRAM cell stability is based on the N-Curve. The N-Curve method is used to calculate the Noise Margins [8]. The setup for its measurement is shown in Fig. 5. The BL, $\overline{BL}$ and WL are clamped to V_{DD}. A voltage source is applied to the $\overline{X}$ node and is swept from zero to V_{DD}. The current through this node is measured and plotted. The current plot crosses x-axis in three points, say A, B and C. B is called the Metastable point. The difference between points A and B indicates the maximum tolerable DC noise voltage at the $\overline{X}$ node before its contents changes. This is called the Static Voltage Noise Margin [8]. And the difference between between points B and C is the Write Trip Voltage which is defined as the voltage drop needed to flip the internal node value '1' when both bit lines are clamped to V_{DD} [8]. The additional current information provided by the N-curve, namely the peak current located between point A and B, can also be used to characterize the cell read stability. This current metric is the Static Current Noise Margin (SINM) [8]. It is defined as the maximum value of DC current that can be injected in the SRAM cell before its content changes. The current peak between point B and C or the Write Trip Current (WTI) is the amount of current needed to write the cell when both bit lines are kept at V_{DD} [8]. This is the current margin for which the cell content changes. The lower the absolute WTI, the higher the write trip point of the cell [8].

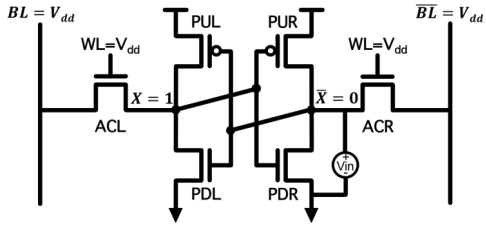


Fig. 5 : Setup for N-Curve Measurement [8]

B. *Active Leakage Current* [9]

The Active leakage current is the amount of current that is consumed by any functional block during the active mode [9]. In a SRAM array, the cells which are in active mode consume this current. A lower active leakage current ensures lower power consumption. When technology nodes decrease, the active leakage current increases. The Active Leakage Current can be different for different stored values. This is attributed to the asymmetrical structure of the cell.

C. *Standby Leakage Current* [9]

The Standby leakage current becomes a significant portion of total current consumption as technology node decreases. It comprises of the subthreshold leakage current (I_{sub}) flowing through turned off nMOS and pMOS transistors. It is due to carrier diffusion between source and drain regions of transistor in weak inversion [9-11]. The subthreshold current is exponential and dependent on the gate voltage [9-11]. The Gate Induced Drain Leakage (GIDL) is part of standby leakage and is caused by high field effect in the drain junction of MOS transistors. This leakage is worsened by high drain to body voltage and high drain to gate voltage [9-11]. Another main component of standby leakage current, the junction current (I_{junc}), flows from data 'one' node to the substrate. This current is also called the Reverse-Diode Leakage [9-11] because it flows when the p-n junction between the drain and the bulk is reverse biased. An illustration of the different types of leakage currents, when X is low for 6T SRAM cell is shown in Fig. 6.

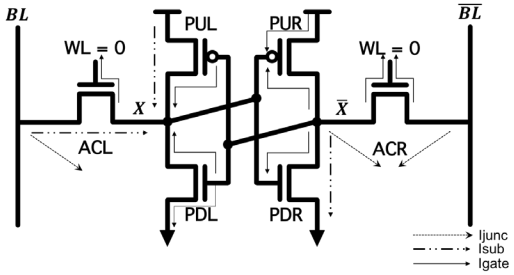


Fig. 6 : Various Leakage Currents in the 6T Cell when X=0 [10]

D. *Read Current* [12]

The current consumed during read operation contributes to power consumption. As such, low read currents are desirable when designing SRAM cells. An illustration for the current flow during read '0' in 6T is shown in Fig. 7. In the figure, the grey coloured arrows show the read current flow through the transistors. The read current in 8T SRAM cell is similar in behavior to the 7T cell. In Fig. 7, it can be observed that the current flowing through ACL and PDL contributes to the read current. Read Currents are negligible while reading value '1' in 7T and 8T cell. This is because R1 is switched off during read and the read bit line remains high, with only leakage current flowing.

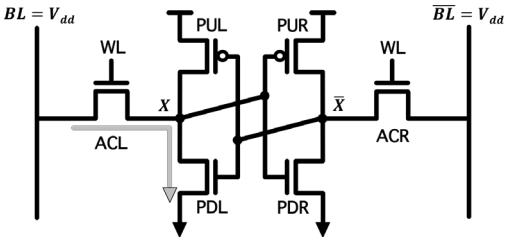


Fig. 7 : The pathway for Read Currents when X=0 in 6T cell [12]

E. *Data Retention Voltage*

The lowest voltage at which an SRAM bit cell retains its bi-stability during standby, and therefore can still preserve its data is known as the Data Retention Voltage (DRV) [13]. A lower supply voltage helps to reduce leakage current. The DRV is the point where SNM is zero i.e. where the butterfly curve collapses. This point on the SNM curve (Butterfly Curve) corresponds to the point B on the N-curve. There are two possible cases in which zero DRV is attained. The first case is when in a symmetric cell the SNM for holding '1', SNM-high (SNMH) and '0', SNM-low (SNML) are the same. When the supply voltage is reduced in such a case, both SNML and SNMH are reduced equally until the butterfly curve collapses, leaving a single metastable point at which both nodes contain the same value. The second case is for asymmetric cells, in which the SNMH and SNML are different to begin with. When the supply voltage is decreased in such a case, the SNM collapses faster for one than the other until bi-stability is lost [13].

IV. Simulation Results

In this Section, the 6T, 7T, 8T and 9T cells have been analysed in deep submicron regions and compared on the basis of SVNM, SINM, WTV, Standby Current, Read Current, Leakage Current and DRV. Simulations have been carried out on three technology nodes viz. 22nm, 32nm and 45nm using the Symica EDA Tool. The power supply values for different technology nodes and the aspect ratios of the transistors for various cells are listed in Table I and II respectively.

TABLE I : Supply Voltage for Different Tech. Nodes

Node	22nm	32nm	45nm
V_{DD} (V)	0.7	0.8	0.9

TABLE II : Transistor Sizing

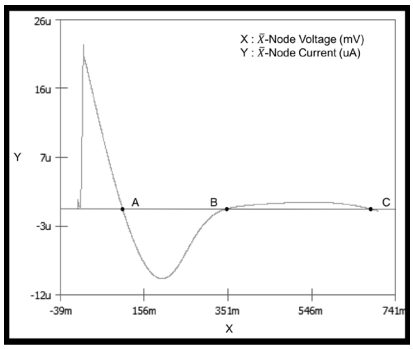
6T Cell			
Transistor	22nm	32nm	45nm
ACL,ACR	36/22	48/32	60/45
PUL,PUR	22/22	32/32	45/45
PDL,PDR	72/22	96/32	120/45
7T Cell			
ACL	48/22	96/32	60/45
PUL,PUR	22/48	32/48	45/45
PDL,PDR	22/22	32/32	120/45
R1,R2	45/22	32/32	45/45
8T Cell			
ACL,ACR	40/22	48/32	65/45
PUL,PUR	22/22	32/32	45/45
PDL,PDR	22/22	32/32	45/45
R1,R2	45/22	48/32	65/45
9T Cell			
ACL,ACR	36/22	64/32	72/45
PUL,PUR	22/36	32/64	45/72
PDL,PDR	22/22	32/32	45/45
RL,RR,R1	48/22	48/32	60/45

A. *Noise Margins*

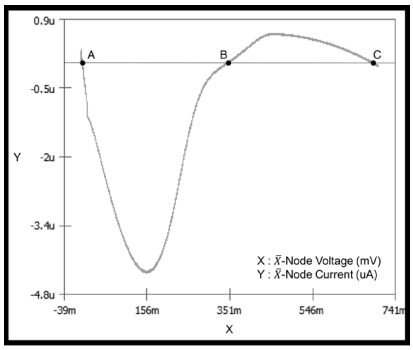
The noise margin for the different SRAM cells is calculated using the N-Curve method. The setup for its measurement is shown in Fig. 5. The current through $\bar{X}$ node is measured for the cells at 22 nm technology node and plotted in Fig. 8. The current plot crosses the x-axis in three points, on the basis of which, noise margins have been calculated and tabulated in Table III. The following observation can be inferred from the results.

TABLE III : NOISE MARGINS

22NM NODE				
	6T	7T	8T	9T
SVNM (mV)	251.44	341.11	358.05	343.63
SINM (uA)	9.78	4.35	5.37	4.72
WTV (mV)	317.94	340.60	323.96	331.80
WTI (uA)	800.24e-3	601.61e-3	2.67	935.05e-3
32NM NODE				
SVNM (mV)	334.48	378.64	385.36	392.97
SINM (uA)	31.91	13.71	14.33	13.72
WTV (mV)	359.04	407.28	402.24	377.60
WTI (uA)	1.54	1.57	4.19	920.91e-3
45NM NODE				
SVNM (mV)	338.67	403.02	421.74	416.14
SINM (uA)	50.54	24.92	25.73	25.11
WTV (mV)	453.72	484.02	464.40	464.20
WTI (uA)	4.29	3.95	8.51	3.25



(a)



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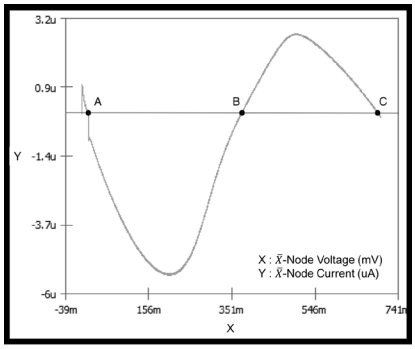
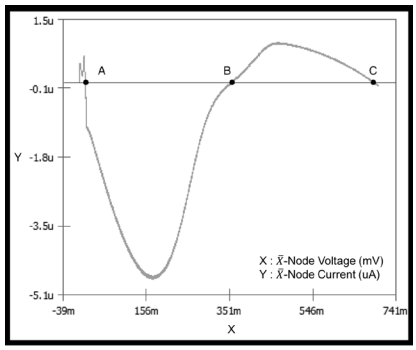


(c)



(d)

Fig. 8 : N-Curves for 22nm tech. node (a) 6T (b) 7T (c) 8T (d) 9T cell

As we scale down, the current needed to read and write into the cell decreases. Both SINM and WTI decrease, thereby decreasing the switching current. The cell with higher SINM, draws more current during the read operation. Any two cells with similar voltage margin can be compared on the basis of current margin. For e.g., in table III, the 7T and 8T cell have similar write margins for 32nm node but the WTI for 8T is much higher than that of the 7T cell. Therefore, the 7T cell is the better performer. The 6T cell showed the worst SVNM across all technology nodes. The 7T cell had the highest Write Trip Voltage across all technology nodes, while the 8T had the highest SVNM across all nodes with the exception of 9T outperforming it on the 32nm technology node.

B. Active Leakage Current

The Active Leakage Current can be different for different stored values. This is attributed to the asymmetrical architecture of the cell. The 7T and 8T cell under consideration in this paper are both asymmetrical with isolated read and write ports. The leakage current also increased with scale down in technology node. Simulation showed that the 7T had the lowest active leakage currents across all technology nodes, while the 6T had the highest.

TABLE IV : ACTIVE LEAKAGE CURRENT

22NM NODE				
	6T	7T	8T	9T
X=0 (nA)	73.48	18.16	40.67	21.46
X=1 (nA)	73.35	38.58	40.34	22.45
32NM NODE				
X=0 (nA)	40.90	10.28	29.85	9.15
X=1 (nA)	41.27	15.18	29.37	9.47
45NM NODE				
X=0 (nA)	24.61	7.55	8.58	5.26
X=1 (nA)	24.31	10.74	8.63	5.19

C. Standby Leakage Current

The standby leakage current was measured for the 6T, 7T, 8T and 9T cells and has been tabulated in Table V. The standby leakage current was highest for 6T cell and lowest for 7T cell across all technology nodes. This is because, it has a single access transistor instead of two as in 8T. The leakage also changed according to the data stored in the cell due to the fact

that the 7T and 8T have asymmetrical structures. Leakage increased with decrease in technology node. However, the 45nm node also gave rise to higher leakage due to its higher supply voltage. The 9T cell had similar leakage during storage of both '0' and '1' due to its symmetrical structure.

TABLE V : STANDBY LEAKAGE CURRENT

22NM NODE				
	6T	7T	8T	9T
X=0 (nA)	74.05	39.21	64.04	29.36
X=1 (nA)	73.86	36.58	40.84	30.49
32NM NODE				
X=0 (nA)	40.09	17.59	23.89	16.37
X=1 (nA)	40.09	14.29	21.87	16.79
45NM NODE				
X=0 (nA)	67.26	31.13	22.35	26.22
X=1 (nA)	66.12	13.44	15.65	26.16

D. Read Current

Read current in 6T is the amount of current that flows through ACL and PDL during a read operation. Read currents are negligible while reading value '1' in 7T and 8T across all technology nodes. This is because R1 is switched off during read and the read bit line remains high. Leakage current flows in this situation. Read currents decreased when tech. node was scaled down. This is due to the inherent size reduction of transistors. The 6T drew the highest currents during the read operation while 7T and 8T the lowest. This can be attributed to the fact that both 7T and 8T have the same architecture for the read port.

TABLE VI : READ CURRENT

22NM NODE				
	6T	7T	8T	9T
X=0 (uA)	13.74	5.86	5.86	7.97
X=1 (uA)	13.74	1.54e-3	1.49e-3	7.98
32NM NODE				
X=0 (uA)	28.74	7.39	7.96	12.37
X=1 (uA)	28.74	1.67e-3	2.46e-3	12.36
45NM NODE				
X=0 (uA)	40.15	12.82	13.45	17.94
X=1 (uA)	40.15	2.38e-3	3.86e-3	18.04

E. Data Retention Voltage

In this paper, all the cells under study are symmetric in nature. The DRV is highest for 6T cell across all technology nodes, while it is lowest for 7T cell. A lower data retention voltage is preferred because it aids in reducing the static power consumption.

TABLE VII : DATA RETENTION VOLTAGE (MV)

	6T	7T	8T	9T
22nm	355.88	344.19	371.77	355.99
32nm	423.92	381.76	392.72	398.06
45nm	434.97	406.53	429.39	419.10

V. CONCLUSION

A comparative study of different transistor configurations viz. 6T, 7T, 8T and 9T SRAM cell in deep submicron region is presented in this paper. The 6T cell provided the least static voltage read and write margin. It also had the highest active leakage current, standby leakage current and read current across all technology nodes. The data retention voltage was the highest of all the four configurations compared. Both 8T and 9T had much better noise margins, lower leakage currents and higher retention voltages in comparison to the 6T cell. However, the best performance was exhibited by the 7T cell. It provided the highest write margins. The static voltage noise margins were second only to the 8T cell. It also had the lowest active and standby leakage currents, lowest data retention voltage and lowest read currents across all technology nodes.

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