On the Implementation of PFSCL Adders

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***Abstract*— In this paper, implementation of full adders in positive feedback source-coupled logic style (PFSCL) is proposed. Three new architectures for PFSCL full adders are put forward. The first architecture is implemented by using conventional NOR based method. The second architecture is based on the use of configurable cell while the last architecture optimizes the structure by using both the conventional NOR and configurable cell based approaches. The functionality of the proposed architectures is verified through simulations by using TSMC 180 nm CMOS technology parameter on Tanner EDA. Their performance is compared in terms of transistor count, gate count, power, delay and power-delay product. It is found that the Arch-3 presents the best PFSCL full adder design by incorporating the advantageous features of the other two proposed architectures.**

Keywords: mixed-signal, digital, PFSCL, configurable cell, full adders.

I. INTRODUCTION

The increasing prominence of mixed-signal integrated circuits have led to rapid and innovative developments in low noise digital circuit design in recent years. The traditional static CMOS logic style with its favorable characteristics such as design ease, rail-to-rail output and negligible static power consumption fails to satisfy the low noise requirement pose in these systems. CMOS circuits generate large switching currents which get coupled to the analog circuits operating on the same substrate thereby degrading the resolution. In literature many techniques to reduce the coupling of the noise has been suggested at various levels [1-4]. Different circuit styles maintaining a constant current source are presented in literature. Positive feedback source-coupled logic (PFSCL) style is one among these style employed in the digital system design due to its high speed characteristic.

PFSCL is an improved version of single-ended source-coupled logic style [5-6]. It involves a positive feedback for speed enhancement. In literature various digital circuits such as serial multiplexer, linear feedback shift register have been implemented but no effort has been made towards the realization of full adder in this style, an essential circuit element for all computations [9-11]. This paper focuses on the implementation of full adder in PFSCL style. Three architectures are proposed and the efficient architecture is identified through simulations.

The paper first describes the basic architecture of PFSCL style and design method for logic function realization in section II. Thereafter, the subsequent section propose three PFSCL based architectures of full adder. Their functionality is verified through simulations by using 180 nm CMOS technology parameters in section IV. A performance comparison with respect to power, delay is also carried out and the best architecture is identified.
Lastly, the conclusions are drawn in V section.

II. PFSCL STYLE

The PFSCL style is a single-ended source coupled logic style employed in the design of mixed signal integrated systems [5]. The style use a constant current source to reduce the switching current generated during signal transitions which degrades the resolution of the on-chip analog circuits. During transitions, the bias current is steered in different branches of the circuit. On this basis, a PFSCL gate has three sections named as current source section, pull down network section and the load section [6]. The pull down network implements the functionality and the load performs the current to voltage conversion. An MOS based schematic of an inverter in PFSCL style is shown in Fig. 1. The source coupled transistor (M_1-M_2) models the inverter functionality. The PMOS transistor M_3 biased in the linear region represents the load while transistor M_4 operate as a current source with a bias current I_{ss} value. When input A is high, the bias current flows through M_1 and potential drop occurs at load such that low voltage is generated at Q. Conversely, for low value of A, I_{SS} flows via transistor M_2 and a high output voltage is obtained. It may also be noted that the presence of current source forms the component of static power consumption in PFSCL gates.

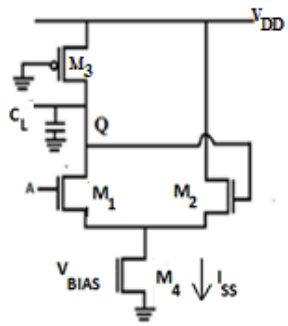

Fig. 1: PFSCL inverter [6]

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The logic function implementation in PFSCL style can be done in two ways. The first one use only NOR/OR gates for function realization due to the inherent advantages of PFSCL NOR/OR gates over PFSCL NAND/AND gates. The other method is based on the use of fundamental cell which can be configured to different functionality and is therefore named as configurable cell. A general discussion on logic implementation based on both of these methods is covered in the rest of the section.

A. NOR gate based approach

The NOR based perception of logic function suggest the use of transistor in parallel since the PFSCL style has only single level source coupled transistor pair in PDN. A generic N-input PFSCL gate is shown in Fig. 2. A NOR based schematic of the two input XOR gate has been represented in Fig. 3.

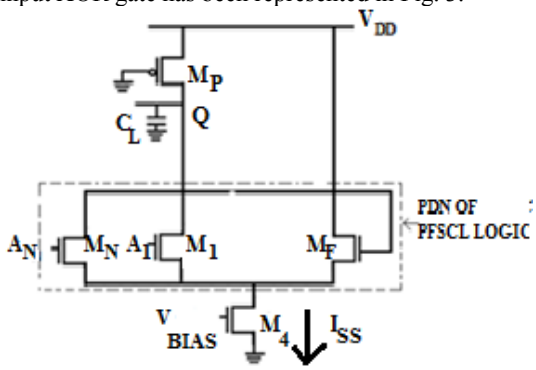


Fig. 2: Generic N-input PFSCL NOR gate

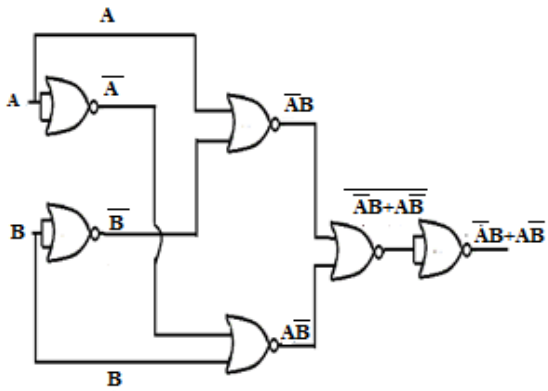


Fig. 3: NOR based schematic of two input XOR gate

B. Configurable Cell based approach [12-16]

This method of logic function implementation use two levels namely a PFSCL inverter and a configurable cell. The cell uses two triple-tail cells (M_3, M_4, M_7) and (M_5, M_6, M_8) biased by two separate current sources of $I_{SS}/2$ [12-16] as shown in Fig. 4a. When input B is high, the transistor M_7 is turned ON, and the transistor M_8 turns OFF so the output is generated according to input A through the transistor pair M_5-M_6. Similarly, when the input B is low transistor pair M_3-M_4 gets activated and the previous output is retained. The aspect ratio of the middle transistors in the triple tail cells is much larger than the other transistors for proper functioning. A block diagram to represent the configurable cell is shown in Fig. 4b. The inputs X1, X2, X3 and X4 forms the inputs of M_5, M_6, M_3, and M_4 respectively. The output nodes Q1, Q2, Q3 and Q4 are attached to each load in the cell. At any instance of time, only one of the two nodes in a triple-tail cell can be chosen for functional realization. The realization of the XOR gate based on this method is shown in Fig. 5.

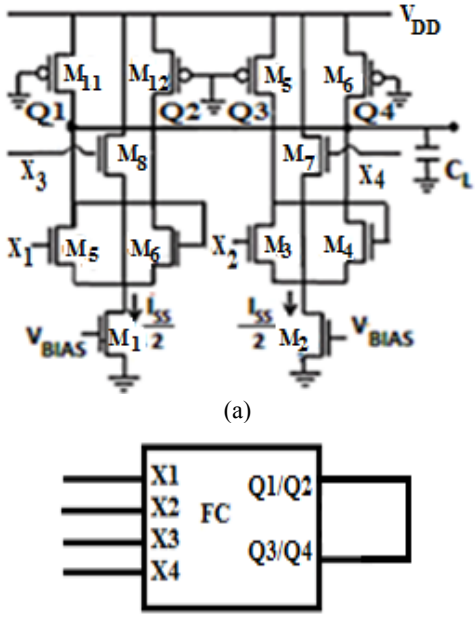


Fig. 4: a) Configurable cell [12] b) Its symbolic representation

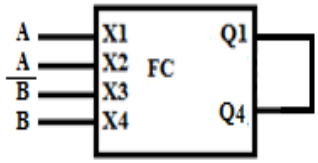
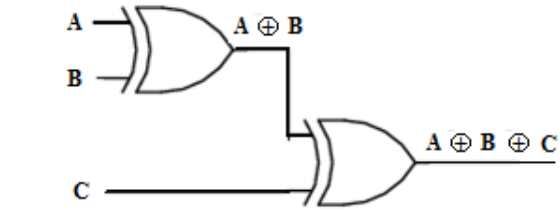


Fig. 5: Configurable cell for XOR functionality

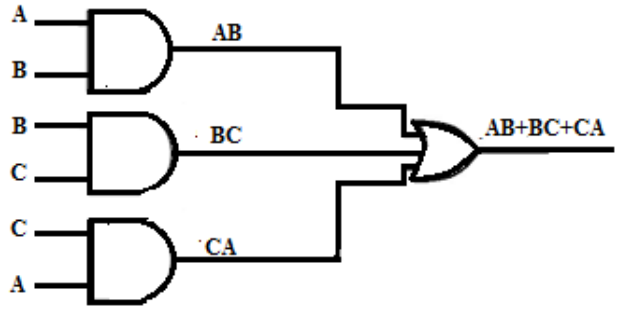
III. PFSCL FULL ADDER

A full adder is a combinational circuit that adds two bits and a CARRY and provides a SUM bit and a CARRY bit as outputs. Various operation such as subtraction, two's complement etc can be performed. The boolean expression to model the functionality of the sum (SUM) and the carry (CARRY) bits are written as eq. (1) and their gate level schematic are shown in Fig. 6.

$$\text{SUM}=A \oplus B \oplus C$$
$$\text{CARRY}=AB + BC + CA \quad (1)$$



(a)



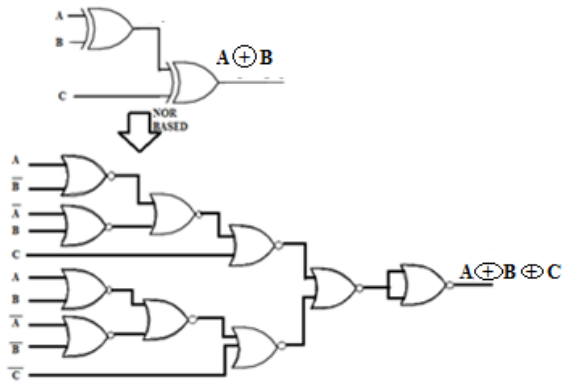
(b)

Fig. 6: Gate level schematic for full adder a) sum circuit b) Carry circuit

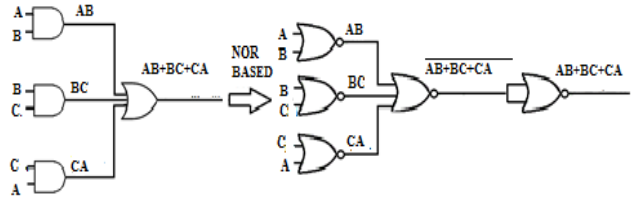
The SUM function involves the use of two 2-input XOR gates while CARRY function is in the form of AND-OR thus requires three AND gates and a single OR gate. Three different architectures to realize the functionality are proposed.

3.1. *Architecture-1 (NOR based full adder implementation)*

The NOR based full adder implementation recommends the use of only PFSCL NOR gates. The SUM expression requires two XOR gate, which is realized by employing PFSCL NOR gate. The gate level schematic is shown in Fig. 7a. In this realization, the D-Morgan's law is used to realize the AND terms such as $\overline{A}B$. The complete gate level schematic of the SUM is drawn in Fig.7a. Based on the same lines, the realization of the full adder CARRY is shown in Fig. 7b.



(a)

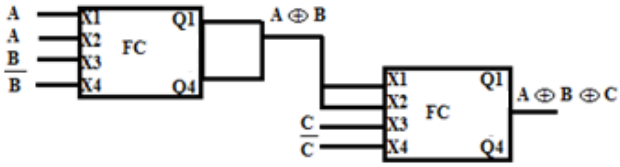


(b)

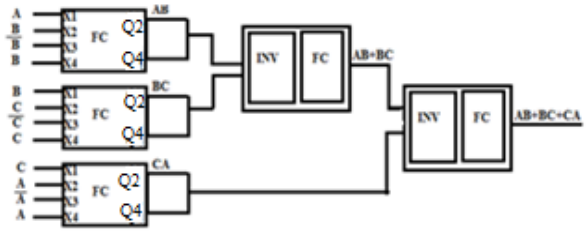
Fig. 7: Proposed Architecture-1 (Arch-1) for full adder (a) SUM (b) CARRY

3.2. *Architecture-2 (Configurable cell based approach)*

The full adder SUM and CARRY realization based on the configurable cell method requires two and five cells respectively. The realization of the SUM by configuring the two cells is shown in Fig. 8a. Each cell in SUM circuit is configured for two input XOR gate. Similarly, to realize the CARRY circuit (Fig. 8b), the configurable cells used in the first level are configured as AND gate while the other levels implements the OR functionality.



(a)

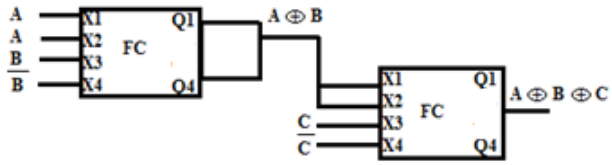


(b)

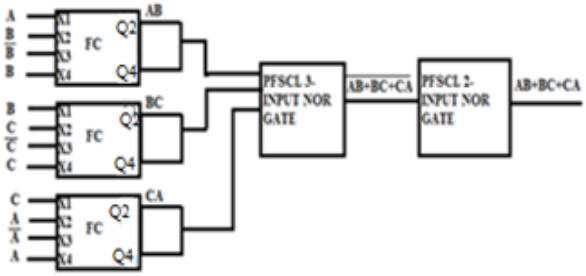
Fig. 8: Proposed Architecture-2 (Arch-2) for full adder (a) SUM (b) CARRY

3.3. *Architecture-3: Hybrid approach*

The basic motivation behind presenting the hybrid architecture comes from the fact that configurable cells lack in implementing NOR functions. On careful examination of the CARRY circuit it can be observed that the last two stages are realizing a three input NOR function and requires two configurable cells. Therefore, the proposed Arch-3 replaces the last two configurable cells in Arch-2 with three input PFSCL NOR gate. The realization of the third architecture is shown in Fig. 9.



(a)



(b)

Fig. 9: Proposed Architecture-3 (Arch-3) for full adder (a) SUM (b) CARRY

IV. SIMULATION SECTION

In this section, the functionality of the proposed architectures of the PFSCL adder is verified through simulations and is followed by a performance comparison. All the simulations are carried out by using TSMC 0.18 µm CMOS technology parameters and a power supply of 1.8 V. A bias current of 100 µA and voltage swing of 400 mV is maintained in the PFSCL gate.

A. Functional Verification

The functionality of the proposed full adder is verified for the above stated simulation conditions. The waveforms of the inputs (A,B,C) and the respective SUM and CARRY outputs obtained from the proposed three architectures (ARCH-1, ARCH-2 and ARCH-3) are shown in Fig. 10. It can be observed that the correct functionality is inhibited by all the proposed architectures.

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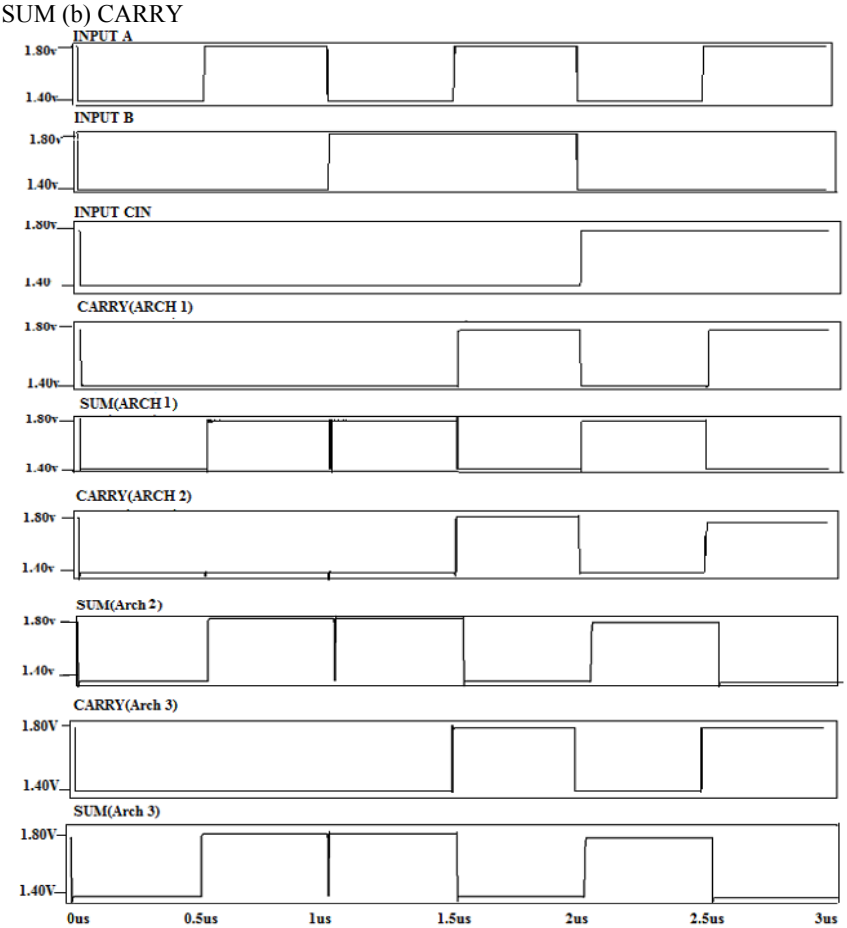

Fig. 10: Waveforms generated from the three proposed architectures

TABLE I: PERFORMANCE COMPARISON

Architecture / Parameter	Proposed Arch-1		Proposed Arch-2		Proposed Arch-3	
	CARRY	*SUM*	*CARRY*	*SUM*	*CARRY*	*SUM*
Transistor count	26	50	68	24	46	24
Gate count	5	10	7	2	5	2
Delay (ns)	4.05	2.73	2.8	0.5	2.2	0.5
Power (mW)	0.9	1.8	1.26	0.36	0.9	0.36
Power delay product (pJ)	3.6	4.9	3.5	0.18	1.98	0.18

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B. Performance Comparison

The performance of the three proposed architectures is compared. A load capacitance of 150 fF is used at the output of SUM and CARRY. The simulation results are summarized in Table I. It is found that the proposed Arch-1 is not efficient as it shows increased value of every performance parameter in comparison to others. This is due to the fact that the use of NOR gates only leads to more number of gates and stages. Alternatively, the proposed Architectures 2 and 3 shows better results. On closer examination, we found that the proposed Arch-3 lowers the transistor count, gate count, power, delay, PDP by 24%, 33.3%, 21.4%, 28.5%, 43.4% respectively in comparison to Arch-2. Similarly, on comparison of Arch-3 performance with Arch-1, beside there is an increase in transistor count and having same power consumption and gate count there is a significant reduction for delay, PDP by 45.6%, 45% respectively. Similar observations are made in SUM circuit. Thus the proposed Arch-3 outperforms the others and can be used in mixed-signal application design.

V.CONCLUSION

This paper proposes three different architectures to implement PFSCL full adders. The first architecture is based on the use of NOR gates in function realization while the second one employs configurable cell. The third architecture is an optimized structure realized by using both the conventional NOR and configurable cell based approaches. The functionality of the proposed architectures is verified through simulations in Tanner EDA. Their performance comparison is carried out between the proposed architectures indicates that the proposed Arch-3 based PFSCL full adder shows a maximum reduction of 45.6%, 45% in delay, PDP respectively over the others.

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