Performance Analysis of Operational Transconductance Amplifier at 180nm Technology

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***Abstract*— This paper presents tutorial on performance analysis for the two-stage CMOS operational transconductance amplifier in conventional gate driven mode. Both the theoretical calculations and computer aided simulation analysis have been given in detail. Designs have been carried out using TSMC 180nm CMOS process. Schematic simulations have been carried out using 'Pyxis Schematic' and simulations have been done using simulator 'Eldo', version 11.2 of Mentor Graphics. Initially DC analysis is performed to find region of operation of all the transistors. Results shows that all the transistors are perfectly operating in saturation region. Further AC analysis demonstrates that Gain of the Op Amp is 75 dB, Phase Margin is 53.8°, & Unity Gain Bandwidth is 30.5MHz Also CMMR is 77.8dB & input referred noise voltage is 0.0fV/√Hz. From transient analysis, slew rate is obtained to be 0.37V/µs, settling time as 472ns. The output swings up to 1.25V and the op-amp dissipates power of 536.5µW under supply voltage of 1.8V. In order to have low power op-amp, supply voltage is scaled to 1.5V & further to 1.2V. The comparative analysis of the results shows that significant saving in power, 18% and 35% respectively, can be obtained without compromising for phase margin & slew rate and little compromise in few characteristics like gain, UGB, and CMRR with supply voltage scaling.**

***Keywords*— Analog circuit; Low voltage low power; Two stage CMOS operational amplifier; Gain; Phase margin.**

I. INTRODUCTION

Over the last few years, there has been tremendous explorations in VLSI industries in response to scaling trends towards deep submicron technology. Demands for low power and efficient portable equipments are rising in day-to-day life. Reduction of supply voltage is common trend for analyzing low power circuits. But in case of metal-oxide semiconductor (MOS) transistor, supply voltage must be at least equal to or greater than the threshold of MOS transistors used in circuit realization. This provides limitations in lowering of voltage supply after certain limit. The rapid scaling of CMOS processes in nanometer demand low supply which helped digital circuit realization at very low power consumption but it is not true for analog circuit realization. The associated drawback is short channel effect which results in low gain stages, decreased impedance etc.

Operational amplifiers are basic elements in many analog processing systems. All the real time signals are analog in nature and hence even if they are processed in digital domain for flexibility and ease of processing, operational amplifiers become a key element in many analog and mixed-signal systems. As the demand for mixed mode integrated circuits increases for low voltage low power operation, the design of analog circuits such as operational amplifiers (op-amps) in CMOS technology becomes more critical [1].

This study aims at studying and addressing various tradeoffs related to performance analysis of conventional two stage CMOS op-amp at deep submicron technology node. In section II, block diagram & fundamentals of two stage CMOS op-amp are discussed. Section III describes topology used and it's working principle. Design considerations are given in Section IV. Also the specifications are clarified and the formula and calculations for design of two stage CMOS op-amp are briefly elaborated. Section V presents the simulation results for various performance parameters & its comparative analysis on performance parameters for conventional gate driven op-amp for various supply voltages & some concluding remarks appear in Section VI.

II. TWO STAGE CMOS OP-AMP

Fig.1 shows basic block diagram of an op-amp. It consists of mainly three stages. As shown in figure 1, the input stage of the op-amp consists of a differential amplifier and it provides the differential to single ended conversion. Normally, a most of the portion of the overall gain is provided by the differential input stage and the second stage is typically an inverter or common source amplifier[2].

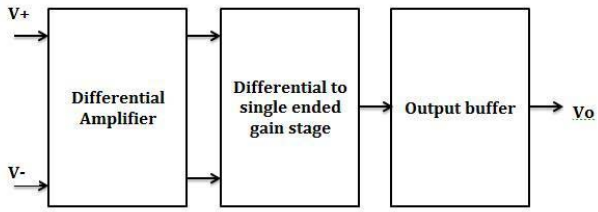

Fig.1 General structure of op-amp [4]

Differential amplifier provides gain ideally up to 40dB, further requirement of gain is accomplished in the second stage. If the op-amp must drive a low resistance load, the second stage must be followed by a buffer stage whose objective is to lower the output resistance and maintain a large signal swing [18]. The output buffer may sometimes be

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omitted to form a high output resistance un-buffered op-amp often referred to as Operational Transconductance Amplifier or an OTA. Those which have the final output buffer stage have a low output resistance and are called as Operational Amplifiers or simply Op-Amp [17].

To establish the proper operating point for each transistor in its quiescent state, bias circuits are provided [2]. Compensation is also externally provided to ensure stability without which op-amp may behave as an oscillator. Ideal op-amp has infinite differential voltage gain, infinite input resistance and zero output resistance. In reality op-amp only approaches these values.

CMOS Operational Amplifier is one of the most versatile and important building blocks in analog circuit design. The primary requirement of an op-amp is to have an open loop gain that is sufficiently large to implement negative feedback concept. The output voltage V_{out} can be expressed as:

$$V_{out} = A_v \times (V_1 - V_2) \quad (1)$$

where, A_v is used to designate the open-loop differential-voltage gain.V_1 and V_2 are the input voltages applied to the non-inverting and inverting terminals, respectively [2].

2.1 Characteristic features of Op-Amp [3]

- **Open loop gain:**

The ratio of change in output voltage to the change in voltage across the input terminals is known as open loop gain of the op-amp. It is also known as differential mode voltage amplification.

- **Common mode gain:**

The ratio of output voltage to the input voltage when both the terminals of the op-amp are supplied same potential is known as common mode gain of op-amp. It is also known as common-mode voltage amplification.

- **Common mode rejection ratio:**

The ratio of differential voltage gain to common-mode voltage gain is known as common mode rejection ratio (CMRR). Ideally this ratio would be infinite with common mode voltages being totally rejected.

- **Slew rate:**

The rate at which the output changes with respect to the time required for a step change in the input is known as slew rate of the op-amp. It is generally expressed in the units of V/μsec.

- **Input common mode voltage range:**

The range of common-mode input voltage that may cause the operational amplifier to cease functioning properly if the input voltage goes beyond this range is known as input common mode voltage range.

- **Unity gain bandwidth:**

The range of frequencies, within which the open-loop g is greater that unity, is referred as the unity gain bandwidth of the op-amp.

- **Total power dissipation:**

The total dc power supplied to the device less any power delivered from the device to a load is known as total power dissipation of the op-amp. At no load,

$$P_D = V_{DD} \times I \quad (2)$$

III. Circuit Schematic Of OTA

The first aspect considered in the design was to select the specifications(specs) to be met. Based on a clear understanding of the specs, the circuit topology of the standard CMOS op-amp was chosen .

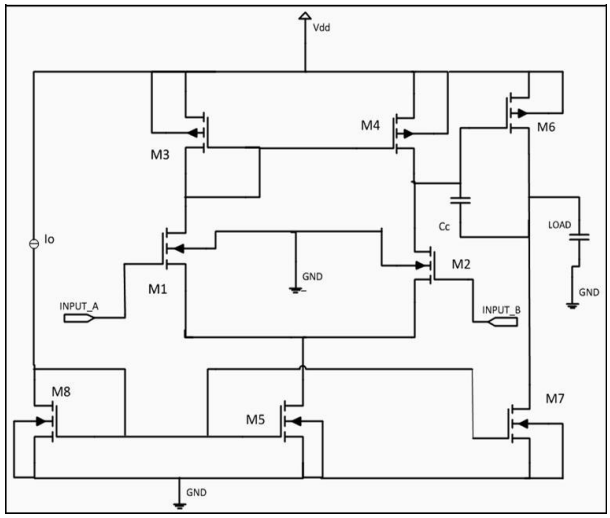

Fig. 2 Unbuffered two stage CMOS OPAMP

As shown in fig.2, it is two stage unbuffered gate driven operational transconductance amplifier where input is applied from the conventional gate terminal of NMOS transistors M1 and M2. Along with M1 & M2, M3 and M4 acting as current mirror load, forms first stage of the operational amplifier. M6 and M7 represent the second gain stage of amplifier. M5 and M8 comprise biasing circuit and Cc represents the compensating capacitance. This two stage op-amp, OTA shown in fig. 2 is widely used because of its structure and robustness.

An ideal op-amp having a single- ended output is characterized by a differential input, infinite voltage gain, infinite input resistance and zero output resistance [18]. In reality op-amp however these characteristics cannot be generated but their performance has to be sufficiently good for the circuit behavior to closely approximate the characters of an ideal op-amp in most applications. With the introduction of each new generation of CMOS technologies design of op-amps continues to pose further challenges as the supply

voltages and transistor channel lengths scale down. Hence in this work main aim is to design the OTA in 180nm technology and to do the performance analysis of various characteristics.

IV. Design Considerations Of OTA

For the design of analog circuits, it is mandatory to have specifications for its customization. Specifications are divided into two categories. First is circuit specification which is given by the designer or manufacturer for its design, and second is EDA tool specification which is provided by the EDA tool vendor.

4.1 Circuit Specifications:

- Supply Voltage, V_{DD} = 1.8 V
- Open loop gain, AV =1000 = 60 dB
- Phase Margin = 600
- Load Capacitance, C_L= 2pf
- Maximum Input Common Mode Range, ICMR (+) =1.8V
- Minimum Input Common Mode Range, ICMR (-) = 0.9V
- Slew rate = 20V/µsec
- Power Dissipation < 0.3 mW
- Gain Bandwidth Product, GBW = 30 MHz

4.2 EDA Tool Specifications:

- $\mu_n C_{ox}$ = 221.55µA/V^2
- V_{thn} = 0.37V
- $\mu_p C_{ox}$ = 93.87 µA/ V^2
- V_{thp} = - 0.39V

Designing has been conceived on the basis of fundamental equations which are used for the calculations of aspect ratios.

The DC gain of the first stage is

$$A1 = -\frac{gm2}{gds2+gds4} \quad (3)$$

The DC gain of second stage is

$$A2 = -\frac{gm6}{gds6+gds7} \quad (4)$$

Overall gain of the Op-amp

$$Av = A1.A2 \quad (5)$$

$$Av = \frac{gm1.gm6}{(gds2+gds4)(gds6+gds7)} \quad (6)$$

Slew rate of conventional Op-amp is

$$SR = \frac{I_5}{C_c} \quad (7)$$

Where I_5 is the current through the M5 transistor and it is the bias current of the input stage.

The Gain bandwidth of the Op-amp is

$$GBW = \frac{gm1}{Cc} \quad (8)$$

Power dissipation of Op-amp is given by

$$Pdiss = (I5 + I6) \times (Vdd + |Vss|) \quad (9)$$

Following table-I shows simulation parameters including calculated values of the aspect ratios obtained from the theoretical performance analysis of op-amp using above equations from circuit technology & also the fundamental equations from the CMOS technology.

TABLE-I: Proposed OTA Parameters

Simulation Parameters	Values
V_{DD}	1.8V
Power consumption	373.5µW
Input bias range	20µA
$(W/L)_1$, $(W/L)_2$	6
$(W/L)_3$, $(W/L)_4$	4
$(W/L)_5$, $(W/L)_8$	20
$(W/L)_6$	75
$(W/L)_7$	175

V. Simulation Results

The circuit was simulated using Eldo with BSIM3v3.3 level 53 model based on a TSMC 180 nm CMOS process. The OP AMP operates with the 1.8V power supply and consumes only 536.5µW power. Simulations results for DC, AC and transient analysis are explained in this section for various electrical characteristics.

5.1 DC Analysis

In DC analysis, region of operation of circuit is determined. Here in two stage operational transconductance amplifier, each transistor must be in saturation region. During DC analysis, all AC relevant parts i.e. capacitor, inductor etc are set to zero. This analysis is important for producing characteristics transfer curve as shown in fig. 3

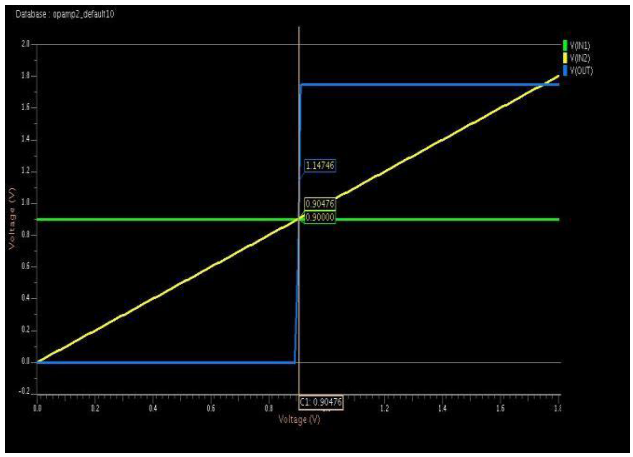

Fig3: DC analysis of op-amp

5.2 AC Analysis

In AC analysis we determine Phase margin, Gain and unity gain bandwidth of the operational amplifier. Both Gain and Phase margin are calculated using DC operating point and AC analysis. The frequencies used to implement AC-analysis are

• Start Frequency = 1 Hz
• Stop Frequency = 1 GHz

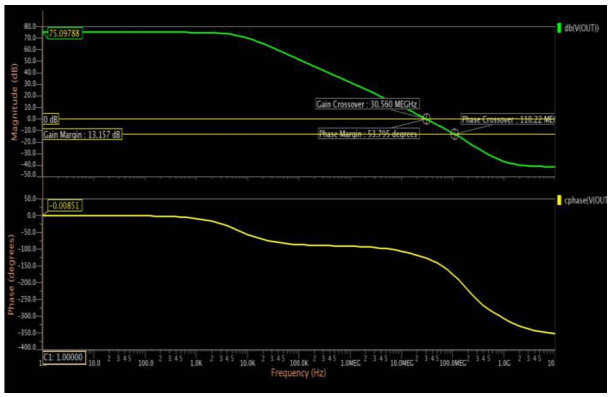

Fig4: AC analysis of op-amp

5.3 Transients Analysis

During transient analysis, first an initial operating point is calculated (based on DC values) and after that all momentary voltages and current are computed as the results of a time dependent well behaved input voltage or current source including the influence of capacitors.

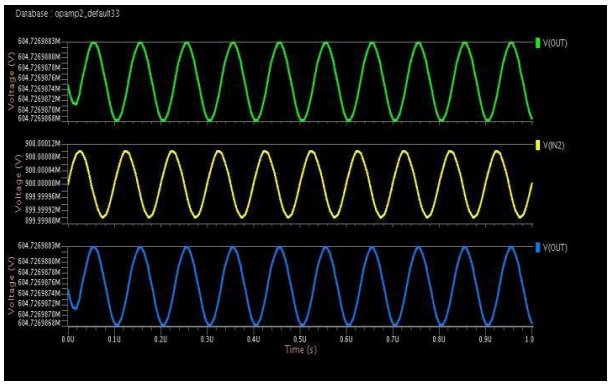

Fig5: Transient analysis of op-amp

5.4 Performance Analysis of designed OTA

The Op-Amp has been designed in a TSMC 180 nm technology with 1.8 V single supply. Simulations have been done using Eldo with a BSIM3v3.3 level 53 transistor model for the TSMC 180nm CMOS technology. Initially it has been assured that all the transistors are operating saturation through DCOP and DC analysis as shown in fig. 3

The phase margin and the open-loop gain of the Op-Amp with a load capacitance C_L =1 pF are depicted in fig4. The DC open-loop gain is 75.1 dB, with a phase margin of 53.8º degrees while the simulated unity gain frequency is 30.56 MHz as shown in fig 4.

The transient analysis shown in fig. 5 also proves the estimated amplitude of the gain obtained in AC analysis. The power dissipation of the simulated operational amplifier is 536.5µW.

Slew-rate (SR) has been obtained by simulation in a non-inverting voltage follower configuration. With a capacitive load of 5pF connected to the amplifier outputs, the measured slew-rate equals 0.37V/µs. Fig. 6 shows the response of the system for a 0.8 V step input signals.

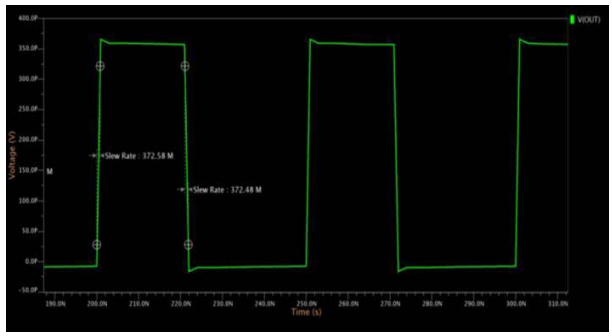

Fig.6: Slew rate of op-amp

Also the settling time is obtained as 270ns as shown in fig.7

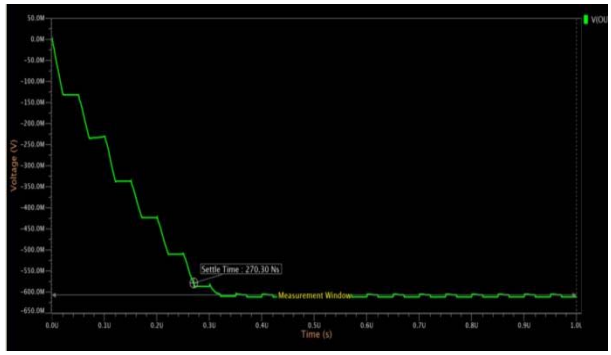

Fig.7: Settling time of op-amp

The simulated input referred noise for C_L= 10 pF is 0.0fV/√Hz for a frequency range from 1Hz to 10GHz, while the simulated output swing of the op-amp in a voltage follower configuration with the same C_L =1 pF connected to each output is 1.75V.

In Fig 8, common mode input voltage Vcm is shown. So the CMRR of op-amp is obtained as 77.8dB.

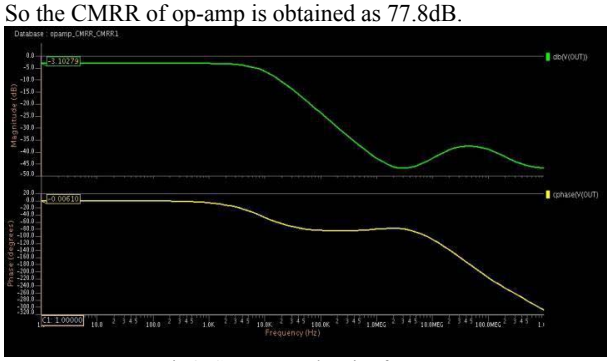

Fig.8: Common mode gain of op-amp

The designed op-amp is also simulated for ICMR. From the DC analysis at the amplifier outputs, the measured ICMR equals 1.05V as shown in fig 9.

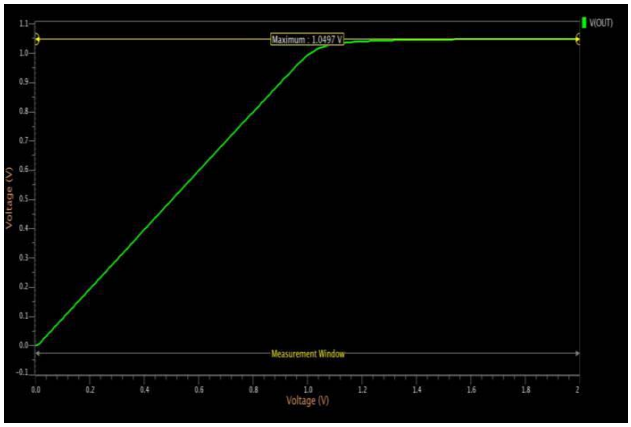

Fig.9: Input Common mode range of op-amp

Similarly input offset voltage is measured to be 0.0µV at the zero crossing point on Y-axis.

The performance analysis of the simulated Op Amp is summarized in Table II, where we also make a comparison between our design specifications and simulated results.

TABLE II: ANALYSIS OF PERFORMANCE PARAMETERS

Sr. No.	Performance Parameter	Design Specifications	Simulation Results
1	Open loop gain	60 dB	75.1 dB
2	Phase margin	60^0	53.8˚
3	Unity Gain bandwidth	30 MHz	30.5 MHz
4	Power Dissipation	< 0.3 mwatt	536.5µW
5	Slew Rate	20V/µsec	0.37V/µsec
6	Settling time	--	270ns
7	Output Swing	1.8V	1.75V
8	CMRR	>= 60 dB	77.8 dB
9	ICMR	1.8V	1.05V

As shown in table II, the simulated results of Op Amp has a power consumption nearly twice than the design specification, achieving best performance characteristics in terms of gain, unity gain bandwidth, common mode rejection ratio, input referred noise voltage, Output swing and better performance for phase margin, slew rate and ICMR.

Since the power consumption is more than the expected, further design verification using low voltage low power strategy is also done. Initially supply voltage is reduced to 1.5V and then up to 1.2V also. Parametric analysis of various tradeoffs of operational amplifier is illustrated with the help of following table III.

TABLE III: PERFORMANCE COMPARISON WITH SUPPLY VOLTAGE SCALING

Supply Voltage → **Performance Parameter↓**	**1.8V**	**1.5V**	**1.2V**
Load capacitance (pF)	5	5	5
Open loop gain (dB)	75.1	74.4	65.27
Phase Margin	53.8˚	53.7˚	54.17˚
Unity Gain bandwidth (MHz)	30.5	30.45	29.24
Power Dissipation (µW)	536.5	443.92	352.77
Slew Rate (V/µs)	0.37	0.37	0.37
CMRR (dB)	77.8	77.2	69.5

From the table III it can be stated that by reducing the supply voltage, significant reduction in power dissipation can be achieved which is very important for power hungry portable applications.

VI. CONCLUSION

A two stage OTA has been realized in TSMC 180 nm technology & it's performance has been analyzed in this paper. Results shows that designed Op-amp meets almost all specifications like a high DC gain 0f 75.1dB, UGB is 30.5 MHz; Phase Margin is 53.8 ˚ and CMRR of 77.7dB. The slew rate of the two stage CMOS op-amp with load capacitance of 5pF is 0.37V/µs with settling time of 270 ns. It also shows the output swing up to 1.75 V with 2pF load and it's ICMR as 1.05V.Simulation shows a power dissipation of 536.5µW for the supply voltage of 1.8V. It is further reduced by the technique of supply voltage scaling. The results shows that significant saving in power is achieved i.e. 18% and 35% for the supply voltage scaling of 1.5V and 1.2V respectively. Also it can be obtained without compromising for phase margin & slew rate and little compromise in few characteristics like gain, UGB, and CMRR. Still power dissipation can be further reduced by operating the transistors in subthreshold region or using bulk driven transistors.

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REFERENCES

[1] Khateb, Fabian, Biolek, Dalibor, Khatib, Nabham and Vavra, Jiri (2010), "Utilizing the Bulk-driven Technique in Analog Circuit Design", 978-1-4244-6613-9/10@2010 IEEE.

[2] Allen, P.E. and Holberg, D.R. (2002), L *CMOS Analog Circuit Design,* New York: Oxford Univ. Press 2002.

[3] Mancini, Ron, *OPAmps for Everyone*, Texas Instruments, August 2002, 11.1-11.22.

[4] Bandyopadhyay, Sayan, Mukherjee, Deep and Chatterjee, Rajdeep (2014), "Design of Two Stage CMOS Operational Amplifier in 180nm Technology with Low Power and High CMRR", *Int. J. of Recent Trends in Engineering & Technology*, Vol. 11, June 2014, ACEEE.

[5] Kargaran, E., Khosrowjerdi, H. and Ghaffarzadegan, K. (2010), "A 1.5 v High Swing Ultra-Low-Power Two Stage CMOS OP-AMP in 0.18 μm Technology", in *Mechanical and Electronics Engineering (ICMEE), 2010 2nd International Conference*, Vol. 1, pp. V1-68–V1-71, 1-3 Aug. 2010, doi: 10.1109/ICMEE.2010.5558594

[6] Kar, Sougata Kumar and Sen, Siddharta (2012), "A Highly Linear CMOS Transconductance Amplifier in 180 nm Process Technology", *Analog Integr Circ Sig Process,* Vol. 72, pp. 163–171, Springer

[7] Luca, M., Francesco, A.A., Felice, C., Gregorio, C. and Giuseppe, I. (2012), "Design of a 75-nW, 0.5V Subthreshold Complementary Metal-oxidesemiconductor Operational Amplifier", *International Journal of Circuit Theory & Applications*, 2012.

[8] Gupta, A., Mishra, D.K., Khatri, R., Chandrawat, U.B.S. and Jain, P. (2010), "A Two Stage and Three Stage CMOS OPAMP with Fast Settling, High DC Gain and Low Power Designed in 180nm Technology," in *Computer Information Systems and Industrial Management Applications (CISIM)*, 2010 International Conference on , pp. 448–453, 8-10 Oct. 2010 doi: 10.1109/CISIM.2010.5643497

[9] Zhang, J.Y. *et al*. (2009), "Design of Low-offset Low-power CMOS Amplifier for Biosensor Application", *J. of Biomedical Science and Engineering*, Vol. 2, pp. 538–542.

[10] Zhang, L., Yu, Z. and He, X. (2009), "Design and Implementation of Ultralow Current-mode Amplifier for Biosensor Applications", *IEEE Transaction on Circuits and Systems II: Express Briefs,* Vol. 56, pp. 540–544, July 2009.

[11] Chatterjee, S., Tsvidis, Y. and Kinget, P. (2005), "0.5V Analog Circuit Techniques and their Application in OTA and Filter Design", *IEEE Journal of Solid State Circuits,* Vol. 40(12), pp. 2373–2387.

[12] Sedighi, B. and Bakhtiar, M.S. (2006), "A New Class AB Current-Mode Circuit for Low-Voltage Applications," in *Circuits and Systems, 2006. APCCAS 2006,* IEEE Asia Pacific Conference, pp. 434–437, 4-7 Dec. 2006.

[13] Mahattanakul, J. (2005), "Design Procedure for Two-Stage CMOS Operational Amplifiers Employing Current Buffer", *IEEE Transactions on Circuits and Systems-II Express Briefs,* Vol. 52, No. II, November 2005.

[14] Ramos, J. and Steyaert, M.SJ. (2004), "Positive Feedback Frequency Compensation for Low Voltage Low Power Three Stage Amplifier," in *IEEE Transactions on Circuits and Systems*, Vol. 51, No. 10, , pp. 1967–1974, Oct, 2004.

[15] Yavari, M., Zare-Hoseini, H., Farazian, M. and Shoaei, O. (2003), "A New Compensation Technique for Two-stage CMOS Operational Transconductanc Aemplifier", in *Proc. IEEE IntI. Conf Electronics, Circuits, Systems, ICECS*, pp. 539–542, Dec. 2003.

[16] Essays, UK. (November 2013). The Most Useful Devices In Analog Electronic Circuitry Engineering Essay. Retrieved from http://www.ukessays.com/essays/engineering/the-most-useful-devicesin-analog-electronic-circuitry-engineering-essay.php?cref=1

[17] Sigroha, Naveen and Krishan, Bal (2015), "A High Bandwidth Low Power Supply CMOS Operational Amplifier", *IJSRD-International Journal for Scientific Research & Development,* Vol. 3, Issue 02, 2015 | ISSN (online): 2321-0613.

[18] Katreepalli, Raghava and Venkateswarlu, Mukku (2012), "Modelling of Operational Amplifier by Using CMOS Technology", *VSRD International Journal of Electrical, Electronics & Communication Engineering*, Vol. 2(6), pp. 330–336.

[19] http://www.physics.unlv.edu/~bill/PHYS483/op_amp_datasheet.pdf

[20] http://lpvo.fe.unilj.si/fileadmin/files/Izobrazevanje/OME/op_amp_datasheet.pdf