Implementation Of High Frequency Fractional Order Differentiator

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Abstract— **In this paper a new approach is suggested for implementing fractional order differentiator in the desired frequency band based on frequency capacitance scaling. The process involves obtaining the rational approximate model of the fractional order differentiator using Matsuda method of approximation and then decomposing it by partial fraction expansion to obtain the circuit parameters (resistance and capacitance). If the frequency band of interest has now to be changed, only the capacitances of the resulting circuit are scaled proportionately. For the choice of the method of approximation and the approach for synthesis, emphasis has been given to accuracy of the model obtained and positive values of resistances and capacitances. The simulations have been performed using OrCAD Capture CIS simulator.**

Keywords- capacitance scaling; fractional order differentiator; Matsuda method.

I. INTRODUCTION

An ideal fractional operator is defined as s^α in the complex s-domain. The values $0 < \alpha < 1$ corresponds to the fractional order differentiator and the values $-1 < \alpha < 0$ corresponds to the fractional order integrator. The general characteristics of an ideal fractional operator is: Magnitude: $20*\alpha$ dB/dec. and Phase: $(\pi/2)*\alpha$ deg [1]. The characteristic features of an ideal fractional order filter cannot be realized with the three passive elements: the resistor, the capacitor and the inductor; because these elements can only reflect the behaviour of integer order filters. Hence, based on electrolytic process or using Lithium Hydrazinium Sulphate as dielectric realizations for fractional order filters is done [2]. The other way to realize fractional order filters is to obtain the integer order approximation [3]. This means a finite integer order transfer function is obtained whose characteristics closely fit the characteristics of an ideal fractional order filter using any of the filter approximation methods [4-9]. Stability, accuracy and order of the integer order model are the factors to be taken into consideration while chosing the rational approximation method. Further the integer order transfer function is decomposed to obtain the circuit parameters using partial fraction expansion or continued fraction expansion. In this way fractional order filter can be realized with the classical circuit elements. However not always the parameters obtained have positive values. In such a case where the circuit elements have negative values, negative impedance converter (NIC) can be used [10]. But the hardware realization becomes more complex as NICs can be built with active elements only. The accuracy of the circuit model lies wholely on the agreement of Laplace model with the characteristics of its ideal counterpart. These circuits which exhibit fractional behaviour are refered to as fractional order element (FOE) or fractance device in literature [11]. The main advantage of using the approach of finite element approximations for realization of fractional order filters is that the simulations required to do the analysis can be performed using the standard circuit simulators and also experimental studies can be done using known circuit elements.

This paper proposes a new simple procedure for implementing the fractional order differentiator in the chosen frequency band of interest, each covering three decades, with the highest frequency band [10^{16} 10^{19}] rad/s. The magnitude and phase characteristics of the transfer function remain unchanged. Also the order of the system obtained is low, which is beneficial for implementation purposes. The design of an efficient circuit of fractional order differentiator, useful in signal processing [12], chaotic systems [13], bioengineering [14] and control systems [15] is made up classical passive elements (resistance and capacitance), connected in such a manner so as to be able to work in a higher frequency range. The number of branches in the circuit depends on the number of poles of the Laplace model. The integer approximation of fractional order filter is obtained by applying Matsuda technique.

The content of the next sections are as follows: Matsuda technique and the basis of scaling a circuit model are discussed in Section II. The design procedure is presented in Section III. The simulations performed and the results are discussed in Section IV and the conclusion is in Section V.

II. MATSUDA TECHNIQUE OF APPROXIMATION AND CIRCUIT SCALING

A. Fractional order Differentiator Applying Matsuda Technique of Approximation.

The Matsuda technique of approximation is based on calculating the gain of the fractional order system at different frequencies and finding a set of coefficients [5]. The

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approximate integer order transfer function is developed for a specific frequency band [f_L f_H] rad/s.
where, f_L is the lower frequency and f_H is the higher frequency.
The frequency points at which the gain is calculated lie within the specific frequency band. Now based on the gain and the coefficients calculated, approximate integer order system is obtained using Continued Fraction Expansion.

The Laplace representation fractional order differentiator is

$$D_f(s) = s^{\alpha}; (0 < \alpha < 1) \tag{1}$$

A group of frequencies f_i rad/s, $(1 \le i \le k)$ in the frequency band is chosen, where k is the number of frequencies and $f_L = f_1$ and $f_H = f_k$

The coefficients a_i's are calculated using eqn. (2),

$$a_i = \begin{cases} gain \text{ at } f_i\,; & for\ i = 1 \\ \dfrac{f_i - f_{i-1}}{q_{i-1}(f_i) - q_{i-1}(f_{i-1})}; & for\ i = 2,3,\dots,k \end{cases} \tag{2}$$

where $q_1(f_i)$ is the gain at $i = 1,2,3,\dots,k$; and $q_2, q_3, \dots q_k$ are obtained as

$$q_2(f_i) = \frac{f_i - f_1}{q_1(f_i) - q_1(f_1)} \quad for\ \ i = 2,3,\dots,k$$

$$q_3(f_i) = \frac{f_i - f_2}{q_2(f_i) - q_2(f_2)} \quad for\ \ i = 3,4,\dots,k$$

$$q_4(f_i) = \frac{f_i - f_3}{q_3(f_i) - q_3(f_3)} \quad for\ \ i = 4,5,\dots,k$$

$$\vdots$$

$$q_k(f_i) = \frac{f_i - f_{k-1}}{q_{k-1}(f_i) - q_{k-1}(f_{k-1})} \quad for\ \ i = k \tag{3}$$

The approximate integer order transfer function using the coefficients calculated is of the form

$$G(s) = a_1 + \cfrac{s - f_1}{a_2 + \cfrac{s - f_2}{a_3 + \cfrac{s - f_3}{a_4 + \dots}}} \tag{4}$$

B. Scaling

The frequency response of a fractional order element consisting of resistor (R), inductor (L) and capacitor (C) can be scaled in three different ways. They are:

1) Magnitude scaling: The magnitude plot in the present frequency band is shifted up or down by scaling each component value in the circuit by a factor 'a'. However there is no shift in the phase plot. The new scaled values are: [R′=aR, L′=aL, C′=C/a].

2) Frequency scaling: The magnitude and the phase plot is shifted right or left from the present frequency band by scaling the frequency dependent component values in the circuit by a factor 'b'. The new scaled values are: [R′=R, L′=L/b, C′=C/b].

3) Magnitude and frequency scaling: The magnitude plot is simultaneously shifted up or down in the present frequency band by a factor 'a' and right or left from the present frequency band by a factor 'b' by scaling each component values. However the phase plot is shifted only right or left from the present frequency band by a factor 'b'. The new scaled values are: [R′=aR, L′=(a/b)L, C′=C/(ab)].

The primed ones are the scaled values.

III. Design Procedure

The approximate model of fractional order differentiator for the frequency band [f_L f_H] rad/s obtained using Matsuda method in partial fraction expansion form is:

$$G(s) = A_P + \sum_{i=1}^{n}\left(\frac{sA_i}{(s+p_i)}\right) \tag{5}$$

Equation (5) is analogous to admittance Y(jω) of an RC network. The network consists of a resistor and cascaded RC cells connected in parallel [16] as shown in Fig. 1. The number of branches in the circuit depends on the number of poles of the Laplace model.

$$Y(j\omega) = \frac{1}{R_p} + \sum_{i=1}^{n}\left(\frac{j\omega/R_i}{(j\omega + 1/R_iC_i)}\right) \tag{6}$$

Comparing (5) and (6),

$$\frac{1}{R_p} = A_p\ ,\ \frac{1}{R_i} = A_i \ \text{ and } \ \frac{1}{R_iC_i} = p_i \tag{7}$$

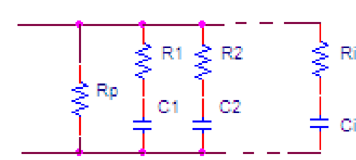

Figure 1. RC circuit model

Now, for the circuit to work in different frequency bands, the value of the capacitances in the circuit are down scaled. The scaling factor for the capacitance is obtained as 10^{-m}, where m is any positive integer depending on the frequency band of interest [f_L*10^m f_H*10^m] rad/s; (f_L is the starting frequency and f_H = f_L* 10^3). The values of all the resistance in the circuit remain unchanged.

Using Matsuda method, the approximate integer order model of fractional order differentiator s^{α} $(0.1 \le \alpha \le 0.9)$ is developed in the partial fraction expansion form (eqn. (1)). The lower and higher frequencies are set as 10^1 rad/s and 10^5 rad/s respectively and k=9. Then the circuit resistances and capacitances according to eqn. (7) are obtained for the value of $\alpha = 0.1$ as shown in Table I.

TABLE I. CIRCUIT RESISTANCES & CAPACITANCES FOR FRACTIONAL ORDER DIFFERENTIATOR S^{α} ($\alpha = 0.1$) IN THE FREQUENCY BAND [10^1 10^4]

s^{α}	$s^{0.1}$
$R_p(\Omega)$	0.9163
$R_1(\Omega)$	0.9273
$R_2(\Omega)$	1.7050
$R_3(\Omega)$	2.2232
$R_4(\Omega)$	2.2676
C_1(mF)	0.0144
C_2(mF)	0.1440
C_3(mF)	1.4000
C_4(mF)	23.300

IV. SIMULATION RESULTS

Using the resistor and capacitor values obtained in Table 1, the magnitude and phase plots of the 0.1-differentiator $s^{0.1}$ obtained from the simulations using OrCAD Capture CIS simulator is shown in Fig. 2. It is seen that the plot exhibits 2dB/dec rise and the phase is approximately 9 deg as desired in the frequency range [10^1 10^4] rad/s.

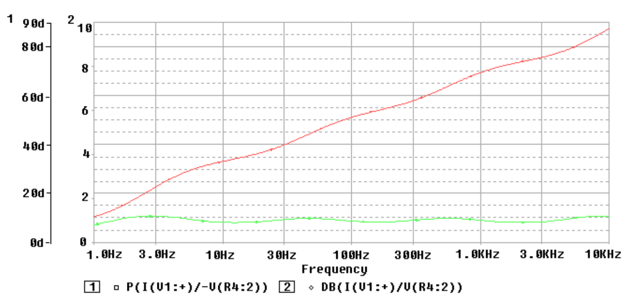

Figure 2. Bode plot of 0.1-differentiator s^{α} (α=0.1) in the frequency band [10^1 10^4] obtained using RC values

Now, choosing m=1 the scaled capacitances obtained for 0.1-differentiator $s^{0.1}$ are C_1'=1.4475μF, C_2'=0.0144mF, C_3'=0.14mF and C_4'=2.33mF in the frequency range [10^2 10^5] rad/s. Similarly choosing m= 3, 6, 9, 12 and 15, the scaled values of capacitances are calculated for the frequency range [10^4 10^7], [10^7 10^{10}], [10^{10} 10^{13}], [10^{13} 10^{16}] and [10^{16} 10^{19}] respectively. Simulations with scaled capacitances for 0.1-differentiator $s^{0.1}$ are performed and it was observed that the frequency response plots were in correspondence to the frequency response plots of ideal 0.1-differentiator in the subsequent frequency ranges of three decade widths.

The magnitude and phase plots of 0.1-differentiator $s^{0.1}$ are shown in Figures 3 and 4 respectively. Both the responses are plotted for different frequency bands [10^1 10^4], [10^4 10^7], [10^7 10^{10}], [10^{10} 10^{13}], [10^{13} 10^{16}] and [10^{16} 10^{19}] respectively of 3 decades each ranging from 10^1 to 10^{19}, obtained by scaling of capacitances. It is seen that the plots exhibit 2dB/dec rise in magnitude and approximately 9 deg (phase) in all the different frequency ranges.

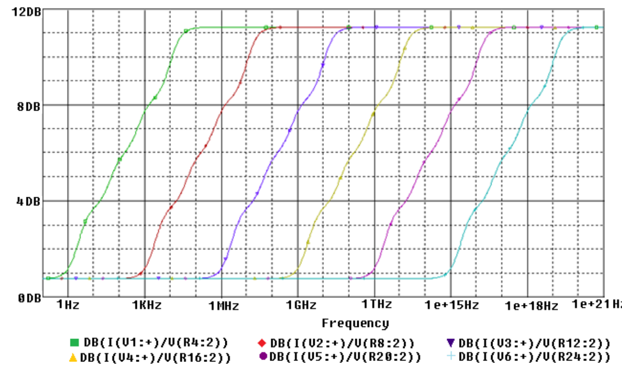

Figure 3. Magnitude plots of 0.1-differentiator s^{α} (α=0.1) for different frequency bands obtained by scaling of capacitances in the frequency band of interest

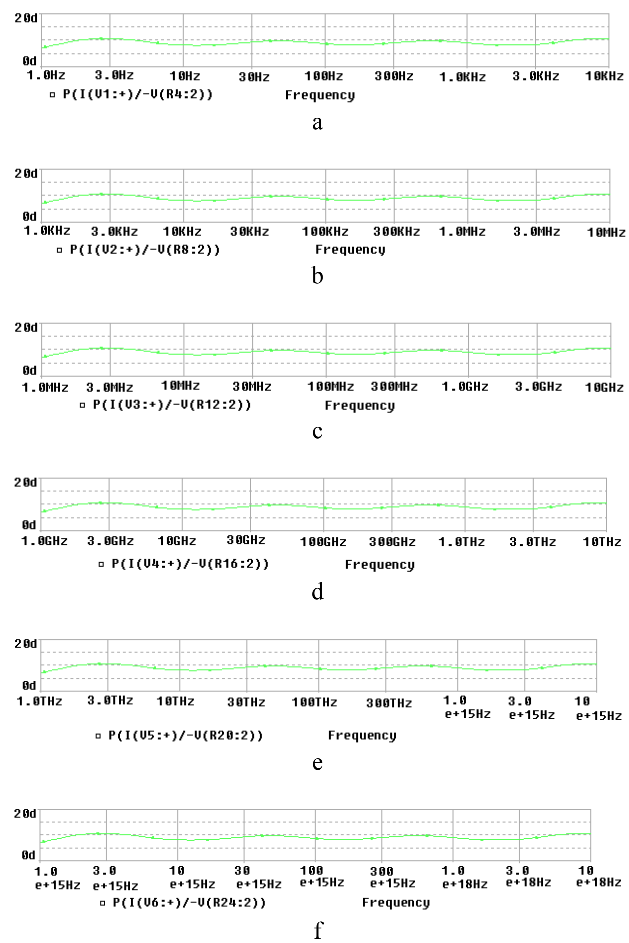

Figure 4. a-f. Phase plots of 0.1-differentiator s^{α} (α=0.1) for different frequency bands [10^1 10^4], [10^4 10^7], [10^7 10^{10}], [10^{10} 10^{13}], [10^{13} 10^{16}] and [10^{16} 10^{19}] obtained by scaling of capacitances

Then simulations are performed for all values of α ($0.1 \le \alpha \le 0.9$) and frequency response plots obtained. It is observed that the magnitude plots exhibit 20α dB / decade rise for all values of α in the range [10^1 10^4] rad/s. Also, phase is correspondingly 90α degrees in each case in the same range. Simulations with scaled capacitances were perfomed and it was observed that frequency plots were in correspondence to the magnitude and phase plots of ideal fractional order differentiators for all values of α in the subsequent frequency ranges of three decade widths.

V. Conclusion

In this paper we have obtained circuit parameters of fractional order differentiator s^{α}. The design procedure adopted here results in passive elements which are all positive as such there is no need of negative impedance converter, hence reducing the complexity of the hardware realization. Also the proposed design method has the following inherent advantages, viz.: the circuit has only one junction with one reference junction and no parameter assumptions have been done. Using the Matsuda method of approximation a vertical shift appears in the magnitude plots in different frequency ranges. This shift can be obtained by multiplying gain of G(s) by a factor of $2^{10 \alpha m}$. These results validate the effectiveness of the proposed work and may be used for realization purposes.

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