Diminution of Power in A Non-Volatile SG DG FinFET based 6T SRAM Cell

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Abstract- In this paper we presented a Shorted Gate (SG) Double Gate (DG) FinFET based 6T SRAM Cell which is non-volatile in nature. For providing the non-volatility a new circuit element called Memristor is used. Memristor signifies the missing relation between the charge and flux among the conventional elements. It retains its previous state even in the condition of sudden power failure. Now-a-days as power is an important consideration for any of the circuit therefore Memristor can be considered as a better candidate for diminution of power. For further reducing the power and other related parameters some power reduction techniques like MTCMOS and Gated-V_{dd} are also applied. The simulations were carried out for conventional SG DG FinFET cell based 6T SRAM cell with Proposed SG DG FinFET based 6T SRAM Cell with Memristors. The techniques applied also shows significant reduction in parameters, like Static power consumption reduces from 42.035 pico-Watt(pW)(conventional circuit) to 40.75 pW(proposed circuit) and goes to 0.423 pW (gated-Vdd).

Keywords— Memristor; Memristance; Non-volatile FinFET; Power Consumption; MTCMOS; Gated-Vdd.

I. INTRODUCTION

With CMOS technologies approaching the scaling ceiling, FinFET's have replaced the present technologies in nanometre regime. SRAM's are widely employed for mobile applications, because of their simplicity and low standby leakage. In recent years the need for low power devices has been escalating immensely. This demand may be due to fast development of battery operated portable appliances such as cell phones, laptops and other handheld devices. But also at same time trouble arising from continuous technology scaling has recently made power reduction a vital design concern for digital circuits.

The paper here describes SRAM cell through double gate (DG) FinFET [1] and highlights the essential improvement in terms of power consumption. Double gate FinFET may be employed using several design types such as shorted gate (SG) and independent gate (IG) [2].

The two gates on either side can be coupled, this switches the FinFET ON or OFF. Double gate FinFET has greater scalability and good cut-off characteristics [3]. Basically, FinFET is designed by means of thin fins which serves as a body which provides ease in conduction and reduces Short Channel Effects (SCE) [4, 5]. Regardless of the following advantages suppose that here the system is failed to recover its state, mainly after an unpredicted power failure, then the Non-volatile logic enables to store/restore states during power on/off operations without the risk of data loss or the consumption of additional time and power [6, 7]. A concept known as non-volatile FinFET (nvFinFET) has been proposed which not only enables chips to attain low power consumption for store operations, but also attain fast power on/off processes and reliable operation even in the event/condition of sudden power failure. It is therefore essential to explore emerging devices for building memory that have lower power dissipation, higher performance, higher density and reliable operation for future computing systems. For providing the non volatility, Memristors are taken into account. The memristor is a new building block for electrical circuits, an addition to the family of "passive" devices that also includes the resistor, the capacitor and the inductor. This device is basically a resistor with varying resistance, dependent on the history of the device. It can be used for memory, where the data is stored as a resistance [8]. Thus it can serve as a memory.

This element can be flipped ON with the current in one direction and OFF with the current in the reverse direction. In this work we would analyze the SRAM cell using non-volatile SG Double Gate FinFET. The paper starts off with the description of memristor and its characteristics followed by the introduction. After that some related works were discussed. Then it goes straight into the structure of

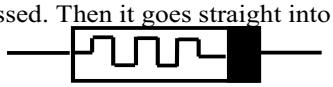

Fig.1. It shows the memristor symbol. In general, it is

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asymmetric and we use the following convention when possible: when a positive voltage is applied to the terminal denoted by the black thick line with respect to the simple terminal, the memory device goes into a state of low resistance.

our proposed circuit, its working principle, then it discusses the perspectives, draws some comparisons, and finally conclusion is drawn.

II. MODELLING OF MEMRISTORS

The memristor is a device which acts as a variable resistance and "remembers" how much amount of current has flowed through it, by altering the voltage across its terminals. The symbol of memristor is shown in Fig. 1. The memristor is regarded as the fourth fundamental circuit element that relates between the charge (q) and the flux (φ) as shown in Fig. 2. The existence of the memristor was first postulated by Prof. Leon Chua in1971 [9] and later generalized to memristive systems in1976 and many potential applications were also reported, e.g., the memories for low cost technology [10], [11], programmable logic [12] and reconfigurable logic [13].

This simple structure allow the devices to scaled down to < 10 nm in size without suffering from the same problems facing transistor scaling [14].The memristor is a very small device that can be split into two main parts:

I) a low doped region with high resistance (R_{OFF}).

II) a high doped region with low resistance (R_{ON}).

Moreover, the memristor has the ability to retain its state for a long time even after the current has been switched OFF. Strukov et al. [15] presented a physical model of the Memristor that is illustrated in Fig. 3. They used a very thin film Ti_{O2}, sandwiched between two Platinum (Pt) contacts and one side of the Ti_{O2} is doped with oxygen vacancies, which are positively charged ions. Therefore, there are two thin films, one is undoped and the other is doped. This doping process makes two different resistances i.e. high resistance (undoped) and low resistance (doped). The semiconductor thin film has a definite length D and the internal state variable w. Thus, the mathematical model for memristive device resistance is described as –

The memristor is properly defined as a two-terminal element in which the flux linkage φ_m between the terminals is a function of the amount of electric charge q that has passed through the device.

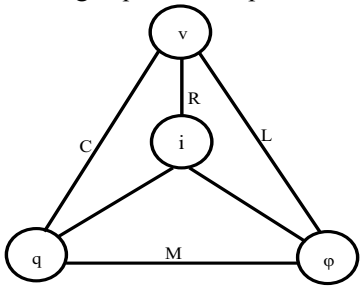

Fig. 2 Relationship between Four Fundamental Quantities

Each memristor is depicted by its function relating the rate of change of flux with respective to charge.

$$\mathbf{M(q)} = \frac{\mathbf{d\varphi_m}}{\mathbf{dq}} \quad (1)$$

Observing from Faraday's law of induction that magnetic flux is basically the time integral of voltage and charge is the time integral of current, we may note down the more convenient form as-

$$\mathbf{M(q(t))} = \frac{\frac{\mathbf{d\varphi_m}}{\mathbf{dt}}}{\frac{\mathbf{dq}}{\mathbf{dt}}} = \frac{\mathbf{V(t)}}{\mathbf{I(t)}} \quad (2)$$

It can be inferred from this that memristance's resistance is simply charge-dependent.

If,

$$M\ (q\ (t)) = \text{constant}$$

then we obtain Ohm's Law,

$$R\ (t) = V\ (t)/\ I\ (t) \quad (3)$$

Although M(q(t)) is important, but the equation is not alike because q (t) and M (q (t)) will differ with time. Resolving for voltage as a function of time we obtain

$$\mathbf{V(t) = M(q(t)).I(t)} \quad (4)$$

where,

$$\mathbf{M(t) = Ron\frac{w(t)}{D} + Roff\ (1 - \frac{w(t)}{D})}$$

This equation reveals that memristance defines a linear relationship between current and voltage, as long as charge does not change. The power consumption attribute recalls that of a resistor i.e. I^2R.

$$\mathbf{P(t) = I(t)V(t) = I^2(t)M(q(t))} \quad (5)$$

As long as M(q(t)) varies little, such as in alternating current, the memristor will emerge as a resistor and if M(q(t)) increases quickly, however, current and power consumption will rapidly stop. Furthermore, the memristor is static if no current is applied. If I (t) = 0, we uncover V (t) = 0 and M (t) is constant.

III. CONVENTIONAL FINFET BASED SIX TRANSISTOR(6T) SRAM CELL

The shorted gate DG FinFET SRAM cell structure is superior choice due to the self-alignment of both gates and the fabrication compatibility with the standard CMOS fabrication technology [16]. The other benefits of FinFET based 6T SRAM cell over

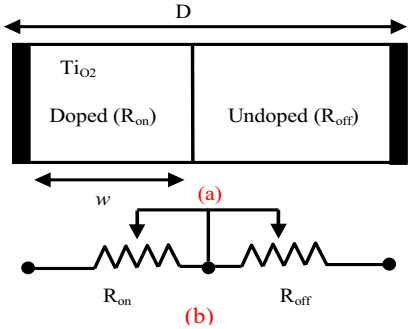

Fig. 3(a & b) Memristor Physical Models.

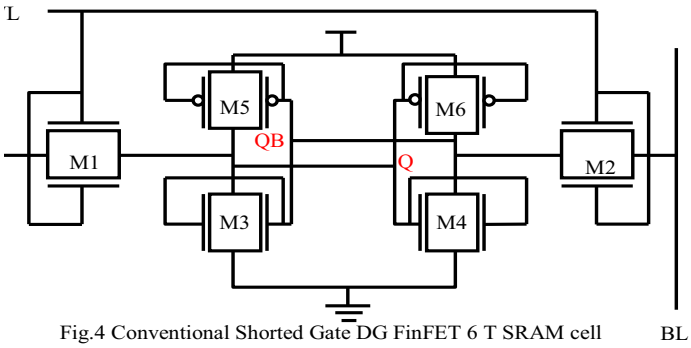

Fig.4 Conventional Shorted Gate DG FinFET 6 T SRAM cell

the existing conventional 6T SRAM cell are Lower leakage, low V_{th} variability due to low channel doping, less variability caused by random dopant. Moreover, it also reduces short channel effects(SCE). The structure of 6T SRAM cell using DG FinFET is shown in Fig. 4. It consists of six SG DG FinFET's in which four DG FinFET's are designed simply by using cross coupled inverters to form a latch (i.e. 2 PMOS and 2NMOS) and two NMOS DG FinFET's transistors which are called as Access Transistors.

These two access transistors serves to control access to the storage cell during read and write operations. The access to the cell is facilitated by the Word Line (WL) which controls the two access transistors M1 and M2 which, in turn, control whether the cell should be connected to the bit lines: Bit Line(BL) and Bit Line Bar (BLB).They are used to perform both read and write operations. There are mainly three operating regions in FinFET based SRAM cell: Hold operation, Write operation and Read operation. All these operations are described below:

In the Hold operation, SRAM is capable of retaining the data as long as it is powered. It means if the word line is disabled (WL = 0), the access transistors (M1 and M2) become off and bit line and bit line bar are disconnected from the latch. The two inverters are cross-coupled and they continue to reinforce each other as long as they are connected to the supply voltage (V_{dd}).

The Read and Write operation depends on the WL and two bit lines BL and BLB. For the period in which WL is at high (say, V_{dd} = 0.7 V), the access transistors M1 and M2 becomes 'ON' and allow access to the storage nodes 'Q' and 'QB'.

For the write operation, both the bit lines are at opposite voltages i.e. if BL is high, then BLB will be its complement i.e. BL=1,BLB=0 or BL=0,BLB=1 and when WL enables transistors M1 and M2, the data will be written on the nodes Q and QB.

Similarly, read operation of this cell is inverted of the write operation. For read operation, both bit lines are at high voltage, and WL is raised to high. Since one of the nodes is low, one of the pre-charged bit lines start discharging and at that instant data can be read at the time of discharging. A sense amplifier is connected to the output node to read the changing value. Therefore read and write cycle is performed.

IV. PROPOSED MEMRISTOR BASED CIRCUIT

Here we proposed a non-volatile FinFET cell i.e. an SG DG FinFET cell which consists of two non-volatile cell i.e. Memristors (MR1 and MR2). The proposed circuit is shown in Fig 5. The conventional FinFET cell is modified to implement the non-volatile functionality by incorporating two Memristors. The Memristor based FinFET cell also consists of two access transistor and two pull-down transistors. The working is same as the conventional one, but in addition here Memristors show changes in resistivity along the direction of low frequency current flow. The Memristors here are allied in opposite directions for making them into high bias condition and low bias condition. Two Pmos devices of a FinFET cell flow current in the forward direction when power is applied making one Memristor in the high bias state. By making a cell discharge all the way through power lines for power down events, one of the Memristor will flow current in the reverse direction. The Memristor will have the low bias state during the power off period. The resistivity mismatch between the two current paths is used for information storage. The directions for current flow are also mentioned in Fig.5. The mismatch will bring back the data stored just before the power down. When the power is on, the load device of the current path having the low bias state will have higher voltage than that of the other path having the high bias state. The latch mechanism of the FinFET cell instantly recovers the original data before the power down. Circuit simulations examine the possibility of circuit malfunction due to this resistivity mismatch. About 2 to 3 % changes may occur. The effect of resistivity changes in the memristor will be practically negligible. Here the

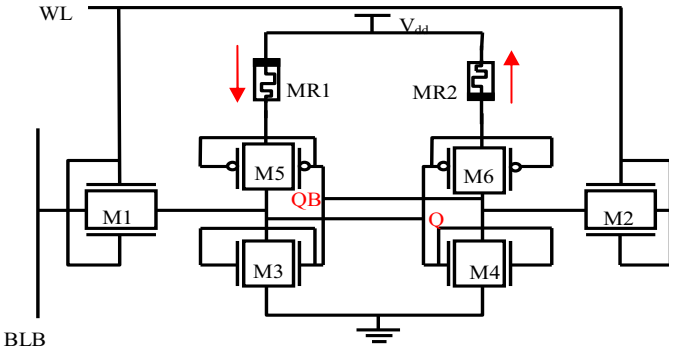

Fig.5 Memristor based SG DG FinFET based 6T SRAM cell.

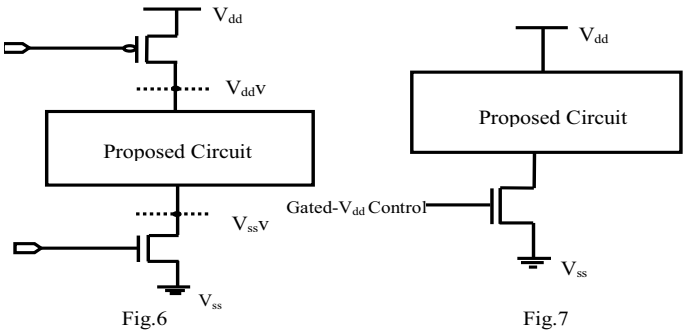

Fig.6 Fig.7

Fig.6 and Fig. 7 shows FinFET cell with MTCMOS and Gated-V_{dd} Scheme.

Memristors used, prevail over the disadvantages of Conventional FinFET, mainly it provides the non-volatile characteristics to the Conventional circuit and thus offer shorter booting time, and thereby consume less energy and power.

V. POWER REDUCTION TECHNIQUES

The suggested FinFET based 6T SRAM cell with Memristors diminishes power to a significant level but for additional diminution in power, two power reduction techniques are applied.

A. MTCMOS Circuit Technology

MTCMOS mainly known as Multi-Threshold Voltage CMOS Technology [17] has appeared as an increasingly prevalent technique to reduce leakage power during the standby mode, though achieving high speed in the active mode. It is proposed to fulfil both requirements of high-speed and low-power. This MTCMOS technology has two key features:

1) Nmos and Pmos with two different threshold voltages are employed in a single chip.

2) It has two operational modes, "active" and "sleep," for proficient power management.

Fig.6 shows the essential MTCMOS circuit scheme with the Proposed SG DG FinFET based 6T SRAM cell. The power terminals are not allied directly to the power supply lines V_{dd} and V_{ss}, but rather to the "virtual" power supply lines $V_{dd}v$ and $V_{ss}v$.

The real and virtual power lines are linked by transistors M5 and M6. These have a high threshold voltage of about 0.35-0.45 V which serve as sleep control transistors. Signals **SL** (Sleep) and **SLB** (Sleep Bar), which are associated to the gates of M5 and M6, respectively used for active/sleep mode control.

B. Gated V_{dd} Technique

As the technology is scaling Leakage power has been increasing exponentially [18]-[19]. Power-gating or Gated- V_{dd} technique is one of the most effective standby-leakage reduction method recently developed [20]-[24]. In a power gating shut off power supplies. It is shown in Fig. 7.

A sleep transistor can be either a pMOS or nMOS high V_{th} transistor that connects permanent power supply to circuit power supply which is commonly called "virtual power supply".

Using nMOS gated-V_{dd} transistors, however, significantly diminishes standby energy dissipation through the stacking effect of three nMOS transistors between the bit-lines and ground. Gated-V_{dd} maintains the performance advantages of lower supply and threshold voltages while reducing leakage and leakage energy dissipation. The essential reason for the diminution in leakage is the stacking effect of self reverse-biasing series-connected transistors [25].Gated-V_{dd}'s extra transistor produces the stacking effect in conjunction with the SRAM cell transistors when the gated-V_{dd} transistor is turned off.

To confirm the outcomes, simulations were carried out which reveals noteworthy diminution as shown.

VI. SIMULATION VERIFICATIONS

A. *Power Consumption-*

Power consumption is now the major technical problem facing the semiconductor industry [26].With the growing use of portable and wireless electronic systems decrease in power consumption has become one of the main concerns in today's and system design. For a digital circuit, the overall power consumption includes two components and it can be expressed as-

$$\mathbf{P_{total} = P_{dyn} + P_{static}} \quad (6)$$

where,

P_{dyn} = Dynamic power consumption

P_{static} = Static power consumption.

1) Dynamic Power :

The average dynamic power consumption ($\mathbf{P_{dyn}}$) is given by-

$$\mathbf{P_{dyn} = 1/2 C_L V^2_{dd} \alpha f} \quad (7)$$

Where,

$\mathbf{C_L}$ is the switching capacitance,

$\boldsymbol{\alpha}$ is the switching activity of output node

Table I.

S. No.	Parameters	Notation	Value
1	Process Technology	-	45nm
2	Supply voltage	V_{dd}	0.7v
3	Resistance of the un-doped region	R_{off}	1600
4	Resistance of the doped region	R_{on}	100
5	Dopant mobility	μ	10e-14
6	Length of the memristor	D	10e-9
7	Temperature	T	27°C

Table I shows the Memristor properties, with the help of this table, following parameters are calculated.

And **f** is the operating frequency.

In (7) the $\mathbf{V^2_{dd}}$ factor suggests reducing supply voltage as the most effective way to decrease power consumption, that means halving the voltage will diminish the power consumption by a factor of four.

2) Static Power :

The Static power consumption can be given as –

$$\mathbf{P_{static} = V_{dd} * I_{static}} \quad (8)$$

The static power is due to leakage sources in the transistors, including the gate direct tunnelling leakage and the sub-threshold leakage [27]. Static current is determined by the input signal states. Although dynamic power consumption is weakly coupled with temperature variation, static power consumption is a strong function of temperature [28].

B. Power Dissipation **-**

Power is the product of applied voltage to the circuit and current flow through the circuit due to applied voltage source.

Power (P) = Voltage (V_{dd}) * Current (I_{dd}) (9)

So this indicates us to define two different types of dissipated power -

1) Average Power

Energy consumed by circuit in unit time is known as Average Power [29], which is shown in fig 8 as:

$$\mathbf{P_{avg} = E/T = 1/T} \int_0^T (i_{dd\,(t)} * V_{dd\,(t)}) \quad (10)$$

2) Peak Power

Rate of energy flow in every pulse is called as Peak Power[30].

$$\mathbf{P_{peak}} = \frac{\mathbf{E}}{\Delta \mathbf{t}} \quad (11)$$

The calculation for various power parameters and techniques mentioned above are shown in Table II and graphically in Fig.8 respectively.

VII. CONCLUSION

The memristor has several qualities that make it attractive for memory chips. First, it is non-volatile, so that it remembers its state after electrical current is switched off. Second, it can be scaled to a single nanometer (nm) in size, whereas the one-bit flash memory cell is expected to reach its scaling limit at about 20 nm. Thus, we portrayed a Memristor based SG DG FinFET 6T SRAM cell. Here the memristor elements are used as storage devices. The main disadvantage associated with the SRAM cells and FinFET based SRAM cells is the fact that storage circuits based on this technique cannot retain data, but this problem is also resolved by our proposed nvFinFET SRAM cell. Here the power related parameters are simulated and calculated which shows power reduction as compared to the The circuit is simulated under ideal conditions at 27° C temperature using Cadence virtuoso tool at 45 nm technology.

Table II.

Types of Power	Conventional FinFET cell	Proposed Memristor based FinFET	MTCMOS (in active mode)	MTCMOS (in sleep mode)	Gated V_{dd}
Dynamic Power	5.356nW	4.982 nW	2.350 nW	2.473 nW	2.404 nW
Static Power	22.44 nW	21.68 nW	4.316 nW	4.821 nW	4.17 nW
Average Power	42.0 pW	40.7 pW	0.43 pW	0.57 pW	0.42pW
Peak Power	4.683µW	4.589 µW	0.822 pW	0.842 pW	1.02 µW

Table II. Shows the Dynamic power consumption (in nano-Watt(nW)).

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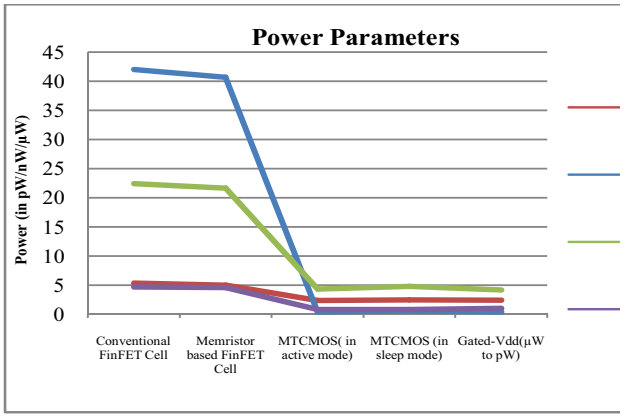

Fig.8 Shows the various Power parameters calculated.