International Conference on Innovative Applications of Computational Intelligence on Power, Energy and Controls with their Impact on Humanity (CIPECH14) 28 & 29 November 2014

Hybrid CMOS-Memristor 4T-NVSRAM Cell for Low Power Applications

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***Abstract*— Introduction to Memristor and Memristive devices in VLSI design and electronics add new features to both analog and digital circuit design. Memristor finds applications in different fields like memories with a non-volatile behaviour (NVRAM- Non-Volatile Random Access Memory), neural networks, robotics to mimic biological entities, Low-power and remote sensing applications, Analog computation and circuit Applications, Crossbar Latches, and Programmable Logic and Signal Processing. The basic property of Memristors is data storage, i.e. it serves as a memory element. This paper presents a hybrid combination of CMOS (Complimentary Metal-oxide Semiconductors) and the memristor to design a non-volatile load 4-Transistor (4T) Static Random Access Memory (SRAM) cell for Low Power applications. By combining the flexibility of MOS devices and the non-volatility of Memristors, storage circuitry shows potential to realize highly power-efficient and non-volatile storage systems. Memristor is a non-volatile element that memorizes the amount of charge passed through it while storing the information in the form of resistance. Simulations demonstrate the utility and functionality of the circuitry, where the memristor is precisely modeled using CAD tools. Simulation results are performed on Cadence virtuoso tool at 45nm technology. The results show that the proposed SRAM cell has the optimized results at a resistance of 10MΩ. The proposed circuit has Static Power (4.89X10^{-9}Watts), Dynamic Power (5.09X10^{-8}Watts) and Average Power (2.79X10^{-8}Watts).**

Keywords— Memristor; Non-volatile memory; semiconductor memory; low power; Emerging technology;

I. INTRODUCTION

Memories have played the role of the main ingredient of most of the digital electronic devices. As the size of the chip gets reduced, it increases the number of transistors with system complexity which requires much more power to operate the system. So, power consumption becomes a major problem for designers. So, there is a need to minimize the power consumption of the memory for improving the system's performance, its efficiency and stability. Static Random Access Memories (SRAMs) are the volatile memories that are unable to retain their data when get powered off. Non-volatile memories preferred as strong candidates, which can be completely power cut without losing any data. In non-volatile memory category, flash memory [1] is the most popular one in the market due to the small cell size. However, it could never replace SRAM because of the slow write speed. There is a need to build up a new non-volatile memory that could replace flash memory with comparable yield and high read/write speed. Results presented in [2] show how a resistive RAM system can be employed along with traditional memories (SRAM/DRAM) to reduce leakage power. Several emerging non-volatile (NV) memories are developed in the recent years like ferroelectric memory (FeRAM) [3], magneto-resistive memory (MRAM) [4], phase-change memory (PCM) [5], resistive memory (RRAM) [6] or Memristors, and conductive-bridging memory (CBRAM) [7].

The conventional nanoscale CMOS (nano-CMOS) technologies are approaching their physical limits. Researchers are actively investigating alternative technologies to meet ever increasing computing and mobile demands. Researchers have shown that Memristors are coming forward as an alternate substitute to CMOS transistors based circuitry with the rising demand for high capacity and lower power consumption in memory devices. The CMOS-based memory technologies are facing many problems regarding the demand for faster processing and larger data size. SRAM is the most widely used on-chip semiconductor memory due to its small size and fast access time, but found limits in achieving higher capacity and lowering power consumption. The simple structure, small size and non-volatility of memristor make it a feasible contender for next-generation memory technology. Memristor is categorized under the resistive memories since logic states are encoded in the memristor's resistance [8]. At present, the research interest for designing digital as well analog systems with memristors as core circuit elements [9] have been on an increasing rate. Memristors are helpful in providing programmability to the analog circuits [10]. Different non-volatile SRAM cells were developed based on this hybrid architecture [11] [12]. This non-volatile memory is referred as "hybrid" because it combines the flexibility, reliability and functionality of CMOS devices with the non-volatile behavior of the Memristor device [13]. This hybrid circuit which consists of memristors and CMOS transistors provides either the same or increased functionality to the circuit, in terms of providing the small size, non-volatility

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and low power [14]. Memristors have an advantage that they are easily compatible with CMOS structures over the other emerging memory technologies.

The paper is systematized as follows: Section I contains the overview and working of the basic 4T SRAM cell. Memristor device and its modeling are found under section II. Section III included the proposed SRAM cell using Memristors. Results are simulated in section IV while the conclusion is given under section V.

II. CONVENTIONAL LOAD 4T SRAM CELL

The Static RAM cell which contains Four-transistors and two-resistors (4T-2R) [15] are fit for stand-alone SRAM devices and for medium to high performance applications. The first proposed low power SRAM cell is the 4T SRAM with high resistance [16] cells. High-Resistance cells do not need bulk PMOS due to which the size of the memory cell was smaller than the conventional 6T SRAM cell. The 6T SRAM cell produces a cell size of an order of magnitude larger than that of a DRAM cell, which results in a low memory density. Therefore, conventional SRAM cells that use the 6T SRAM cell have difficulty meeting the growing demand for a larger memory capacity in mobile applications. In response to this requirement, our aim is to design an SRAM cell which uses less area and its power consumption is also reduced with no degradation in performance. So, we designed a 4T SRAM cell (Figure-1). This cell structure uses two high-polysilicon resistors (R1 and R2) as the load in each inverter (replacing the p-channel MOS transistors in the 6T SRAM cell). These high polysilicon resistive loads are stacked above these transistors [17] for the more compact cell size. The 4T-2R SRAM cell is initially 30 percent smaller but more power hungry and less reliable than 6T SRAM cell. The cell consists of only four NMOS transistors (T1–T4). The 4T-2R SRAM cell, however, is less stable than the 6T SRAM cell. The two NMOS transistors (T3 & T4) act as pass-transistors whose gates are joined to word line and tied the cells to the columns. The remaining other two NMOS transistors (T1 & T2) used as pull-down transistors of the SRAM cell. Instead of its advantage of small size, the 4T cells have several drawbacks. It has a relatively high leakage current and consequently higher standby current.

A. Operation of 4T SRAM Cell:

The 4T-2R SRAM design (Figure-1) comprises of four transistors (T1 to T4) and two resistors (R1 and R2). Transistors T3 and T4 formed two complementary bit lines (BL and BLB). If any one of them is enabled, then either BL (Bit Line) or BLB (Bit Line Bar) will be triggered by V_{CC} and the other one to GND (Ground). This operation is referred to as the reading operation of the SRAM cell. If anyone out of BL or BLB are driven to V_{CC} and vice-versa to GND, then T3 and T4 are enabled, and then disabled, the SRAM cell will remain in the state due to the bit lines. This process is known as write process of the SRAM cell. The 4T-2R SRAM has a definite amount of leakage current from GND to V_{CC}. For this reason, we use transistors with resistors.

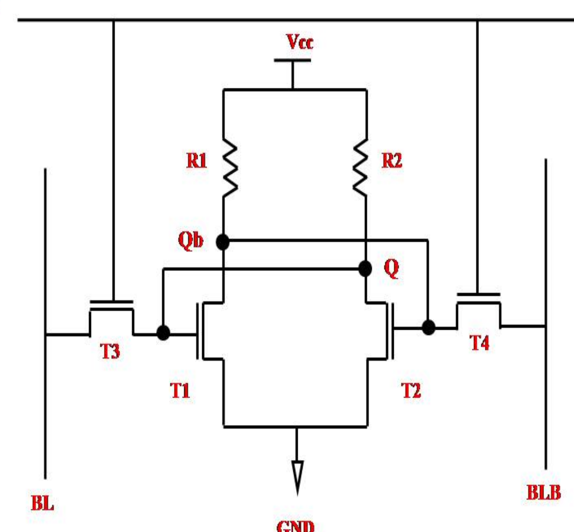

Figure-1 Basic diagram of load 4T SRAM cell

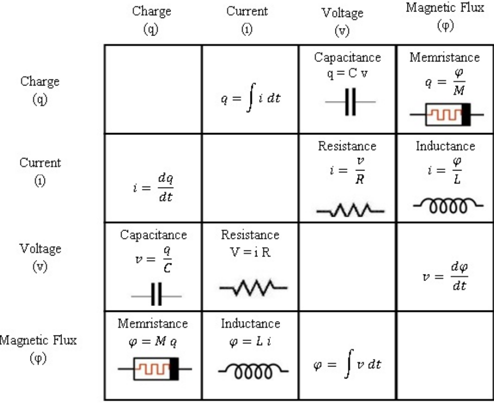

Figure-2 Conceptual symmetry between resistor, capacitor, inductor and Memristor

I. MEMRISTOR DEVICE AND ITS MODELING

Memristor [18] - [20] is a passive element that has resistive memory with two non-volatile resistive states (ON and OFF). The principle to operate it is the symmetry between magnetic flux and the charge. The symmetry diagram between Resistance (dv=Rdi), capacitance (dq=Cdv), inductance (dφ=Ldi) and Memristance (M) is shown in Figure-2. The structure of the memristor is shown in Figure-3 (a). The Memristor is a very small device that can be divided into two main parts: a low doped area with high resistance (R_{off}) and a high doped area with low resistance (R_{on}). Each region had a different resistivity. Thus, Memristance represents this behaviour as two resistors are in series as given by equation 4 and shown in figure 3 (b).

$$R_M (x) = x(t)\, R_{on} + [1- x(t)]\, R_{off} \quad (1)$$

where, function x(t) is the ratio of the width (w(t)) to the physical length (D) of the component, given by

$$x(t) = w(t)/D \quad (2)$$

The "pinched" characteristic is the "fingerprint" of Memristors [21]. They consume very less power as they

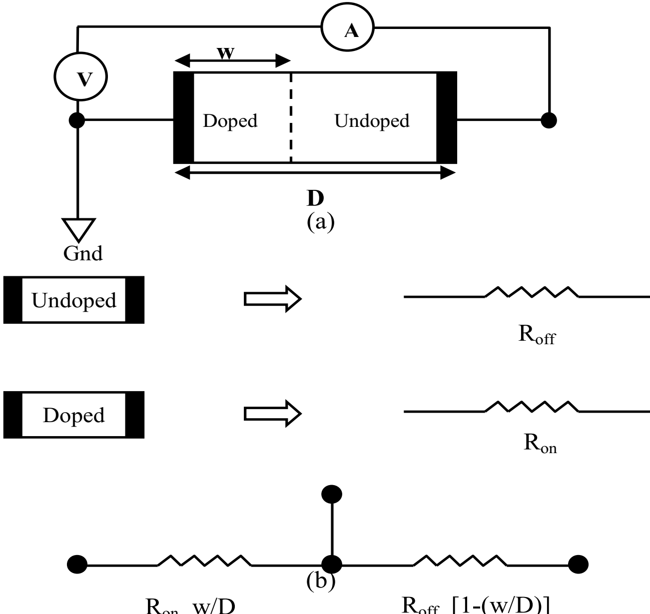

Figure 3 (a) Memristor's device structure (b) Resistance in series

don't need power to retain their state. For the sake of symmetry and completeness, Memristor was formulated by Chua [17] which is characterized by the relationship between the charge (q) and flux (φ) as shown in Figure-2. To model a Memristor, we need to calculate its Memristance (M). Memristance is defined as:

$$M = d\varphi/dq = vdt/idt = v/i \quad (3)$$

representing the expression for the normal resistance following the Ohm's Law. Thus, Memristance defines a linear relationship between current and voltage, as long as M does not vary with charge. Furthermore, the memristor is static if no current is applied. If I(t) = 0, we find V(t) = 0 and M(t) is constant. This is the essence of the memory effect. The power consumption for a resistor is given by:

$$P(t)=I^2R=I(t)V(t)=I^2(t)M(q(t)) \quad (4)$$

II. Proposed Memristor Based Non-Volatile 4T SRAM Cell

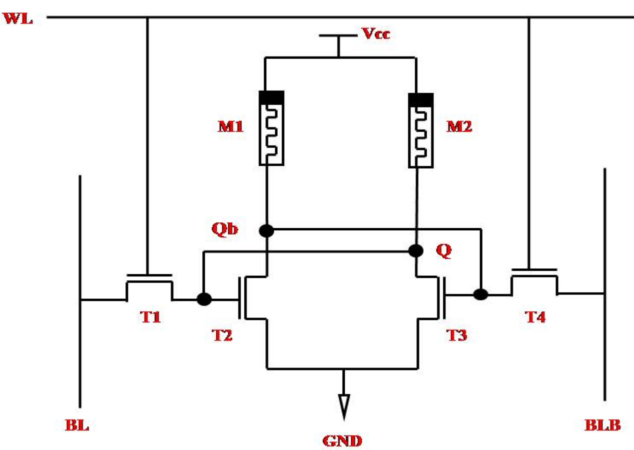

Figure-4 Schematics of memristor based load 4T SRAM cell

The main goal of the manuscript is to design a non-volatile CMOS Static RAM cell with reduced power. With the CMOS scaling, the advances in technology predict that Moore's law found difficulty in its existence. As the size of the chip gets reduced, it increases the number of transistors with system's complexity which requires much more power to operate the system. So, power consumption becomes a major problem for designers. The CMOS-based memory technologies are facing many problems regarding the demand for faster processing and larger data size. SRAM is the most widely used on-chip semiconductor memory due to its small size and fast access time, but found limits in achieving higher capacity and lowering power consumption. Since SRAM cells are volatile in nature. They lost all their data when the power gets turned off. Therefore, researchers and designers are very much interested in memristors in their non-volatile nature with much reduced power. In addition, the progress in utilizing other emerging memory technologies (such as MRAM, and PCRAM) is hindered by their lack of compatibility with CMOS. In order to achieve the non-volatile functionality and low power, two load resistors (R1 and R2) are replaced by memristors (M1 and M2) from the conventional load 4T SRAM cell as shown in Figure-1. Based on different values of resistances, different powers are calculated and noted down. The observations depicted that by using memristors the power also gets reduced. When current flows in the circuit, two load resistors (R1 and R2) memristors comes in the high bias state. During the cell discharge, current flows in reverse direction in one of the memristor of proposed SRAM cell. Memristor is in low state when the supply is off. Between these two current paths, a mismatch is found in the resistivity, which is used for storing the information of the system. This mismatch is responsible for the non-volatile nature too. Data is restored back by this mismatch. When the supply is on, resistor in low bias condition has the higher voltage respective of the other. The original data is recovered immediately by a latch mechanism of the SRAM cell. With increasing the values of resistances, the power gets reduced. The standard value of the load resistor for 4T SRAM cell is 10MΩ.

III. Simulation Results

A Verilog-A model for the memristive device has been developed and used with CMOS circuits for simulation in Spectre. The results obtained here were consistent with the properties of the memristor. The following values were used for simulation: R_{on}=100Ω, R_{off}=1600Ω, D=10 nanometers, μ=10e-14$m^2s^{-1}V^{-1}$, where R_{off} represents the high resistance state, R_{on} represents the low resistance state, D represents the film thickness and μ represents the mobility of dopants in the thin film. When R_{off} and R_{on} were changed, R_{off} represents the peak resistance and R_{on} acts as the initial resistance of the memristor. At an elevated level of R_{off} and R_{on}, the current is found to be low. At low values of Roff, some part of the hysteresis loop is linear with voltage specified, so there is no increment in resistance. This was observed by one of the property: $v(t) = R_{MEM}(w)i(t)$. The relationship is like a

resistance. But the resistance can vary and hence the nature is of nonlinear type.

Power was considered as an important issue, not only in portable devices, but also a significant design constraint in many system designs. Till now, dynamic power has been a major source of power dissipation. However, the static power dissipation consists of a significant portion of the total power. Static power is the power dissipated when no switching occurred into the device and is defined as the product of supply voltage and static current.

A. Static Power Consumption

Static power consumption is the amount of power that is consumed by the unit to retain the data. The static power is also referred to as leakage power in digital circuit design since the static power consumption is due to the leakage current ($I_{leakage}$) passing through the circuit when there is no activity.

$$P_{Static} = P_{leakage} = I_{leakage} \cdot V_{dd} \qquad (5)$$

B. Dynamic Power

Dynamic power consumption of the SRAM unit is especially important when the speed of operation is high.

$$P_{Dynamic} = \alpha f\, C_{interconnect} \cdot V_{dd}^2 \qquad (6)$$

where f is the frequency of operation, $C_{interconnect}$ is the interconnect capacitance and V_{dd} is the supply voltage, which should be taken as 700mV.

C. Average Power

Depending on the design requirements, there are different power dissipation factors that need to be considered. The average power is one of them, which is related to the cooling or battery energy consumption necessities. The average power is defined by the following equation:

$$P_{Average} = \frac{1}{T}\int_0^T (I_{supply}(t) \cdot V_{supply})\,dt \qquad (7)$$

where T is the time duration in seconds, I_{supply} is the current supplied by the circuit, V_{supply} is the supply voltage.

Table I shows the optimized results of 4T-2R SRAM cell at a resistance of 10MΩ. This comparison is shown by a graph represented in Figure-5. Above 10MΩ range in resistances, we found no change in powers of the SRAM cell. So, we took 10MΩ as the standard value of resistance to calculate the optimized result of different powers of 4T-2R SRAM cell.

Table –I
Comparison between basic 4T and Memristor based 4T Non-Volatile SRAM (NVSRAM) cell in terms of Average, Static and Dynamic Power

S.No.	Parameters	Conventional 4T-2R SRAM cell	Memristor based 4T-2R SRAM cell
1	Average Power (Watts)	2.79E-08	5.00E-08
2	Static Power (Watts)	4.89E-09	4.90E-09
3	Dynamic Power (Watts)	5.09E-08	5.10E-08

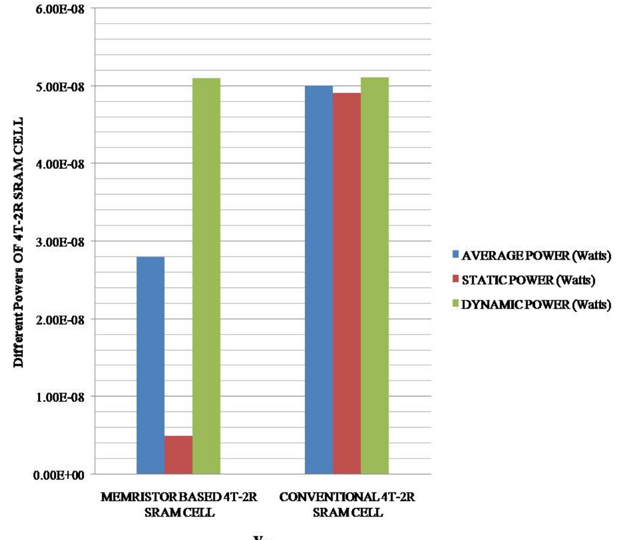

Figure-5 Graph showing optimized results of conventional 4T-2R SRAM cell and the proposed one in terms of different powers

CONCLUSION

In this paper, I have designed and implemented a non-volatile Memristor based 4T-2R SRAM cell. We have also analyzed the power consumption of conventional 4T-2R SRAM cells as well as proposed Memristor based non-volatile 4T-2R SRAM cell. Instead of using a combination of different techniques, a new technology-Memristor is used with the SRAM circuitry. This can result in optimization of low power SRAM that gives better power consumption than any of the deployed techniques. Results showed that Memristor-based 4T-2R SRAM cell gave very much less Power consumption as Static Power (4.89×10^{-9}Watts), Dynamic Power (5.09×10^{-8}Watts) and Average Power (2.79×10^{-8}Watts).

ACKNOWLEDGMENT

This work is supported by ITM University, Gwalior in collaboration with Cadence virtuoso Design System, Bangalore India.

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