Analysis of Low Power Reduction in Voltage Level Shifter

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Abstract— **The preserver for portable devices is satisfied by developing CMOS technology. Voltage level shifter is introduced here using adaptive voltage level technique progression of curtailing the power dissipation and power consumption. Power dissipation is the most important parameter here, the adaptive voltage level technique is apply in present work mitigate the power dissipation. We can reduce the value of total power dissipation by applying the AVLG (adaptive voltage level at ground) technology which is increase the ground potential and AVLS (adaptive voltage level supply) which is raise supply potential. The purpose of the design to investigate the static power and power dissipation for low voltage level shifter for proposed design style. This design is valuable in designing the system that consumes less power. The simulation and performance analysis of proposed circuit evaluate in cadence virtuoso tool. The AVL technique based voltage level shifter compared to conventional design that based on power consumption and power dissipation.**

Index Terms— **AVL scheme, Voltage level shifter, Low power, VLSI circuit**

Introduction

The requirement for the low power and portable device enhancing in large quantities, it is required to scale down the transistor size. For design of low power low power circuit, we have used CMOS VLSI technology and which has accomplished by NMOS and PMOS sub circuit, PMOS device have created with two doped P^+ regions known as drain and source are locate at distance of length, the interface between drain and source terminal known as gate terminal and separated by silicon dioxide (SiO_2) material. NMOS device created by two N^+ regions within a lightly doped p substrate; in the VLSI technology level of leakage power is increase [1].With the large applications of battery supplying devices, such as portable PC, Cellar phones and PDA. Power consumption has taken place a baleful design concern in today's VLSI circuits. Therewith, millions of transistors have grouped into a single chip in nanometer technologies. The heat dissipation due to enormous power consumption occurs a problem that can unfavorably impact on reliability and packaging cost of a design [2].These factors have magnetized much concentration on low power design circuits and campaign large research efforts to address different kind of power reduction technique [3]. An alternative point of view is the multi supply voltage domain technique, consists of distribution to the design into separate voltage domains, each operates at a suitable power supply voltage [4] level depends on its time requirement. Time critical domains drive at higher power supply voltage to maximize the performance, whereas the non critical section drive at lower power supplies voltage to raise the power efficiency [2]. In VLSI technology owing to scaling of transistors leakage power increase, so reduced the power consumption in active mode we are using some reduction technique like Adaptive voltage level at ground (AVLG) and Adaptive voltage level at supply(AVLS) [5].

Circuit Description

A. voltage level shifter

The low power voltage level shifter [6] circuit is configured by three common stages, input inverter, voltage conversion stage and an output stage which is shown in fig.1 below. CMOS circuit is utilized for low power consumption operation; Output inverter is used as inverting buffer. Input inverter is preparing by using Lvt device to offer fast differential low voltage input signal [7]. It is also predicted by using Lvt transistors, the strength of the pull-down network of the voltage conversion stage is also increase. As shown in fig1 differential cascode voltage switch is used in Voltage conversion stage.

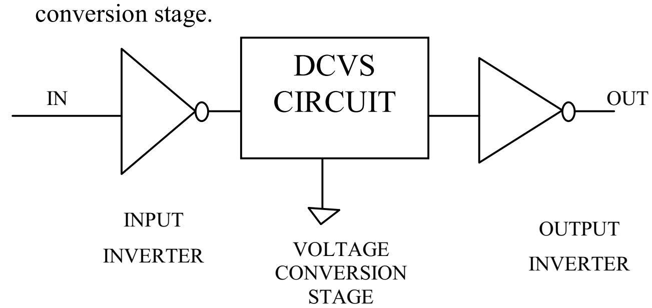

Fig.1 Block diagram of Low Power Voltage Level Shifter

B. Conventional Voltage Level Shifter

The conventional level shifter was considered using 45-nm CMOS technology. The letter confers the designer with Low-threshold voltage (Lvt), Standard threshold voltage (Svt), High threshold voltage (Hvt) [8]. As denoted in figure 2, M4 M5 M6 M7 M8 and M9 are the High threshold voltage transistor, Standard threshold voltage transistor is N4 and remaining transistors are Low threshold voltage transistor. The cross bar current flows from the nodes n and m at initiate to their high-low transition [9] can be concern. Therefore, to decrease these impacts two Lvt PMOS devices (M2, M3) accomplished, M4, M5 preferred as Hvt transistors. This improves in emasculate the pull-up networks of voltage conversion stage, thus decreasing conflict at n, m nodes.

This selection of transistors also moderate the leakage current [10] flows via the pull-up network, when they are turns off. Two diodes are connecting with Hvt PMOS devices (M6, M7) place between pull-up logic and supply VDD_H for ensures consistent voltage conversion. These devices are not only bound the pull-up strength but also control to significant reduce static power. We are illuminating the distinction between the conventional architecture and conventional DCVS. M4 turns ON, because of high-low transition of the core input. The diode moves by the drain current, which connects M6 in the saturation region [11]. There voltage drop (i.e. Vth, M6) generates across M6 terminals that produces a correspondent bulk-source voltage drop on M4, that increases the threshold voltage due to the bulk effect. On the source terminal of M4 bounds its V_{gs} with reduced voltage level (VDD_H-V_{th}, M6), due to this M4 action is weak. All the above effects are reducing the conflicts from the node n so allowing faster discharging to be accomplished.

When M4 is turn on then M5 is automatically turn off. In this case, M5 is not sufficient to turn ON M7 because of small leakage current flow.

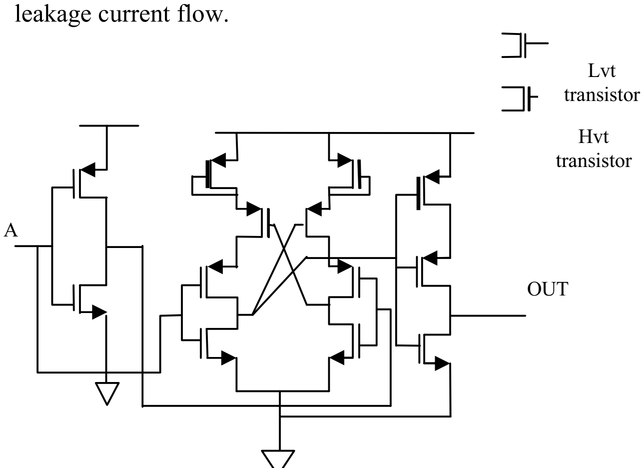

Fig. 2.Schematic of conventional low power voltage level shifter

For this purpose, M5 results power gated from the VDD_H, leading to a considerable reduction in its sub-threshold current [9]. The diode connected M7 device being a factor to minimize the leakage current, also increasing the threshold leakage current because of bulk effect

In view of, M6 limits the output range of conversion stage to (0V,VDD_H-V_{tp}), an output inverter is connecting to node n, to make certain a rail conversion. The pull-down network of an inverter affects a Svt device and pull-up network is modeled by developing Hvt Pmos transistors stack. When n is high, the leakage current is flowing through the pull-up network of the output inverter. M6, M8-M9 can substantial and reverse threshold voltage variations on the latter transistors to go in weak inversion, increase in static power dissipation.

C. Voltage Level Shifter by using Adaptive Voltage Level (AVL)

1) Adaptive voltage level at ground (AVLG): Adaptive voltage level control circuit [12] can be either uses on the upper end of the cell or at the lower end of cell to reduce supply voltage and increase in ground potential (AVLG technique). The effect of these two techniques on leakage current are representing in this section. The leakage current is affected by these two techniques, described in this section.

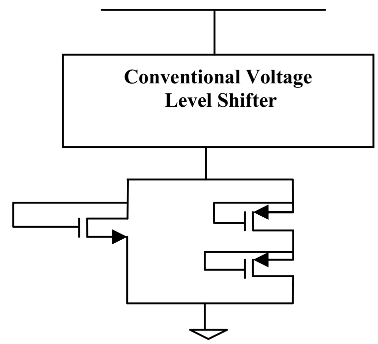

Fig.3 Voltage level shifter using AVLG technique

2) Adaptive voltage level at supply (AVLS) : To summarize the AVLS scheme, use to decrease in the gate leakage current, still leave two gate leakage current components in access transistors unaffected and results in additional sub-threshold leakage current across the other access transistor [13][14]. Figure shows the AVLG scheme in voltage level shifter in 45 nm technology.

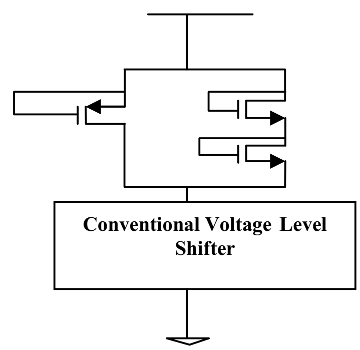

Fig.4 Voltage level shifter using AVLS technique

I. SIMULATION RESULTS

We design a transistor level voltage level shifter circuit using cadence virtuoso tool. In AVLS technique, we have effective percentage reduction in parameter as compared to AVLG technique. The new circuit design simulated and analyzed supply voltage ranges near from 0.7V to 1.2V.

A. Power Analysis

Total power of consumption is the combination of static and dynamic power during on mode, in CMOS Vlsi technology. On the other hand cut-off mode power consumption is due to leakage current in cut-off mode. Dynamic power consumption consists of two mechanisms, first one is switch power and second is short circuit power due to charging or discharging of load capacitance [15] and incomplete rise and fall in input waveforms. The satic power of a CMOS circuit is allocated by the leakage current via each transistor.

1) *Active Power:* When the low power voltage level shifter is on state or working condition, the active power consumption is perform. Basically active power is predictable by giving input voltage and observes the average power consumption [16]. The active power is combination of dynamic and static power consumption [17]. Dynamic power consumption consists of two mechanism, first is the switch power [18] and second one is short circuit power. For calculation of active power, the stop time takes 200ns. Table 1 shows the active power of low power voltage level shifter with AVLG and AVLS techniques and given efficient reduction in active power. The active power calculated by equation [19].

$$P_{active} = P_{dynamic} + P_{static} \quad (1)$$

Where $P_{dynamic}$ is dynamic power and P_{static} is static power due to leakage.

The dynamic power is known by-

$$P_{dynamic} = C_{eff}\, Vdd^2 f \quad (2)$$

Where C $_{eff}$ the switched capacitance, f is is clock frequency. Although [20, 21] consider only the leakage due to I_{subn} and I_{subp} , as [22, 23] points out, the combination of I_j and I_b can be significant.

The static power is known by-

$$P_{static} = Vdd\, I_{subn} + |V_{bs}|\,(I_{jn} + I_{bn}) \quad (3)$$

Where I_{subn}, is Sub-threshold leakage current of NMOS device, I_{jn} is drain to body junction leakage current, I_{bn} is the source to body junction leakage current via NMOS device.

TABLE I. ACTIVE POWER ANALYSIS

Voltage (V)	Active Power in AVLG	Active Power in AVLS
0.7	477.6 pW	32.89 pW
1	1.349 nW	39.79 pW
1.2	2.572 nW	64.05 pW

Now, $$P_{active} = P_{swi} + P_{s\text{-}c} + P_{leak} \quad (4)$$

Where P_{swi} is switching power, $P_{s\text{-}c}$ is short circuit power, P_{leak} is leakage power.

Table 1 shows the active power of voltage level shifter with AVLG and AVLS technique.

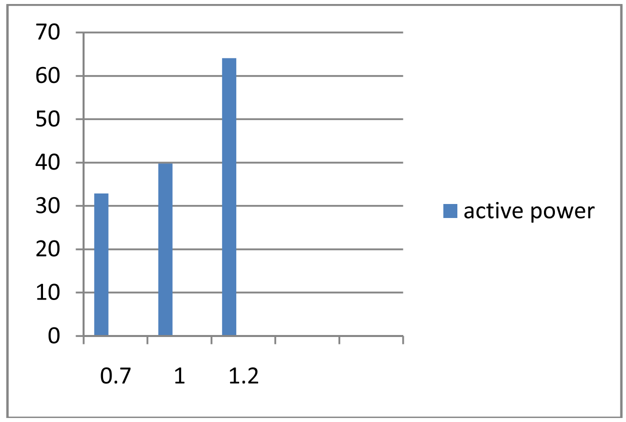

Fig. 5.Active power Graph of AVLS

Fig.5. shows active power graph of AVLS technique at different voltages.

2) *Leakage power:* Leakage power is increase when we reduce the channel length or provide scaling [24]. Leakage power [25] [26] assigns the standby power of any device. Leakage currents are important in burst mode type integrated circuits where most of time the system is in sleep mode. During sleep mode there is no consumption takes place. Leakage current can occur during substrate injection effects and sub-threshold voltage [27].

The leakage power is comprehend by equation-

$$P_{leak} = I_{leak} \cdot V_{dd} \quad (7)$$

Leakage Current: Leakage current of the Low power voltage level shifter evaluated during the standby mode. The leakage current of the low power voltage level shifter, is measured by using NMOS transistor is connected at the pull-down network below the whole circuit. Whenever, the leakage current is calculated, sleep transistor is OFF for this technique [28]. In order to reduce overall power consumption, a well known technique is to scale supply voltages, but this scaling has result exponentially increase in the leakage current [29].The sub threshold leakage current I_{leak} can be approximately formulated as [30].

$$I_{leak} = I_o\, e^{(V_{gs}-V_{th})/\square V_t} \quad (8)$$

and also, Leakage current is derived and calculated by equation given below

$$I_{leak} = I_{sub} + I_{gate\text{-}ox} \quad (9)$$

Where I_{sub} is sub threshold leakage current and $I_{gate\text{-}ox}$ is gate oxide leakage current.

TABLE II. Leakage Parameters Analysis

Parameter	AVLG	AVLS

Leakage Power	90.74 pW	27.88 pW
Leakage Current	46.85 pA	2.38 pA

Table 2 shows leakage parameters of voltage level shifter with AVLG and AVLS. Here AVLS technique is giving better result than AVLG technique.

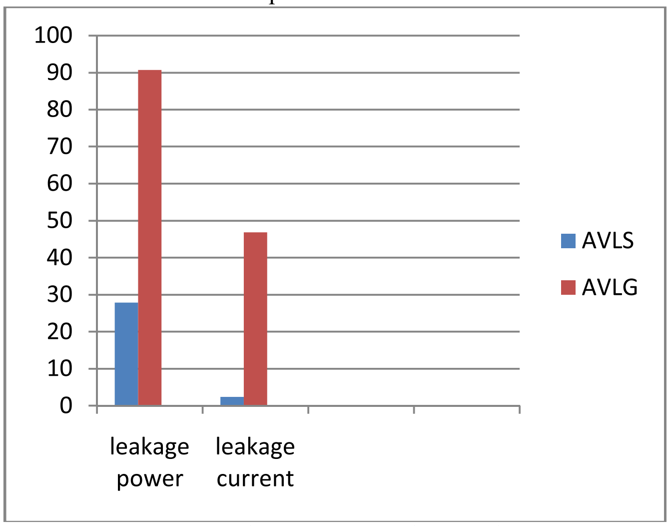

Fig. 6. Leakage Parameter analysis Graph

Fig.6 shows the leakage parameter graph with AVLS and AVLG technique. This graph shows that AVLS technique has more power dissipation as compare to AVLG technique in Voltage Level Shifter.

II. CONCUSION

Voltage level shifter is elaborated using cadence virtuoso tool in 45nm technology, low power requirement of VLSI technology for battery operated circuit is important key factor, so we are configured low power voltage level shifter with AVLG and AVLS techniques for enhancing the circuit parameter like active power, leakage power on nanoscale. AVLS and AVLG techniques have applied in existing work. A simulation result is not only shows better results in AVLS technique but also gives reduction in the power consumption as compared to AVLG technique. An AVL technique Voltage level Shifter is offer reduced threshold leakage power. Simulation result shows that 93% reduction in active power and 69.2 % reduction in leakage power at 0.7V provides by AVLS technique, threshold voltage and input voltage varies from 0.7 to 1.2V. Voltage level shifter, measured result exactly verified the characteristic of low-power circuit. The circuit has been utilized for the design of low power.

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