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Standby and Active Leakage Current Control Mechanism of Half Adder Cell

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***Abstract*—The proposed paper shows the half adder circuit with low power consumption preferred for arithmetic operations. Leakage power dissipation problem of electronics systems has attracted a lot of attention from engineers and researchers over the years. In the CMOS circuits Power dissipation occurs due to increasing leakage current in deep-sub micrometer regimes which is becoming a significant contributor as threshold voltage, channel length, and gate oxide thickness are reduced. The half adder circuit composed of XOR gate and AND logic gate, which have many transistor. Power consumption (leakage power) in the CMOS technology half adder circuit achieving better performance for maintain the speed, power dissipation, size, reliability of the device. SVL (Self-controllable Voltage Level) technique provides better leakage power reduction with minimum area and it not only reduces power but also retains data during stand-by period in half adder. Simulation work has been done in 45 nm technology, in this technology power consumption (leakage power) have provided for half adder circuit.**

***Index Terms*-Half Adder, SVL, Leakage Current, Logic Gate.**

INTRODUCTION

Adders are basic block of computational and many complex arithmetic circuits. In many times a lot of researcher's have attention to arithmetic functions like adder for mobile application. These adders cell commonly aimed to reduce power consumption and increase the speed of operation. In order to meet long battery life for mobile applications, designers have to work within a very tight leakage power specification. Designer's have worry about the portable electronic devices to maximizing battery life with low level of leakage current. For example, mobile phones need to be powered for extended time periods (stand-by mode in which the mobile phone is able to receive an incoming call), but are fully active for much shorter periods (known as active mode, while making a call) [1].

The signal transition or switching, short circuit current which flows from VDD to ground terminal and leakage current are three main sources of power consumption in digital CMOS circuits. That means with the increasing technology, total power dissipation will decrease and at the same time delay varies which is depends upon supply voltage, threshold voltage, oxide thickness, loads capacitance [2].

In the portable battery operated systems, most of the blocks remain idle for longer time of operation. Hence, effective leakage power savings are possible if leakage reduction techniques are applied on a finer block-level granularity. By inserting the power switch transistors, in order to switch off the inactive blocks we can be reduce power efficiently. Self-controllable Voltage Level (SVL) circuit is the most suited for standby leakage power reduction with power switch techniques [3].

For adding, subtracting, multiplying and dividing two bit numbers a combinational digital logic circuit Half Adder is used. A typical adder circuit produces the output, a sum bit and carry bit (denoted by S and C respectively). It can be also realized for adding some other formats like BCD, Ex-3 etc. In address decoder, table formulation, index calculation etc adder circuits can be used for a lot of applications in digital electronics [4] [5] [6]. In digital circuits XOR circuit is basic building block of various circuits like arithmetic circuit adder, multiplier, comparator, parity checker, code converter etc. The block schematic of Half Adder is shown in below figure which has XOR and AND gate for giving output SUM and CARRY respectively.

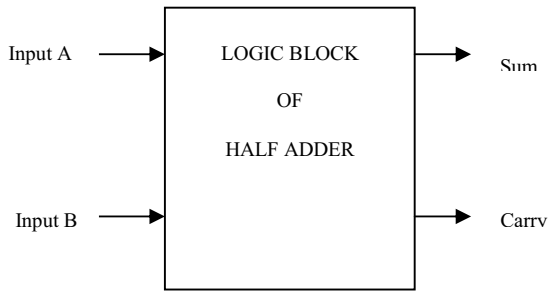

Fig.1. Logic block diagram of half adder

HALF ADDER IMPLEMENTATION USING CMOS TECHNOLOGY

Half adder is a digital electronic circuit that is used to perform addition binary numbers in the processor for most

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application like high speed and low leakage power. Adders are used for not only in arithmetic logic units, but also for address decoding table index calculation in many computers and other type of processors. Adders also have less weigh in terms of silicon area and addition operation [12].

In digital circuit Boolean function where the output is a function of present value is implemented with circuits. Arithmetic logic unit (ALU) is constructed with the help many types of combinational circuits like adder, subtractor, Carry look ahead adder, encoder, multiplexer, decoder etc.

The half adder is core element of basic arithmetic circuits which is used to perform addition of two bit binary input. In the half adder circuit A and B are two inputs and provides SUM, CARRY are two outputs of the circuit. Here SUM bit is the XOR of A and B and CARRY bit is the AND of A and B.

SCHEMATIC REPRESENTATION OF HALF ADDER CIRCUIT

Half adder circuit is a combination of AND gate and XOR gate. The schematic of half adder is drawn by using cadence design software tool. Half adder schematic consists of 18 transistors, in which 9 NMOS and 9 PMOS transistors are used.

The simple half adder circuit design as shown in figure below, in which XOR logic gate represents the SUM and AND logic gate represents the CARRY output.

The addition performs normally four possible elementary operations such as:

0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 0 with carry 1

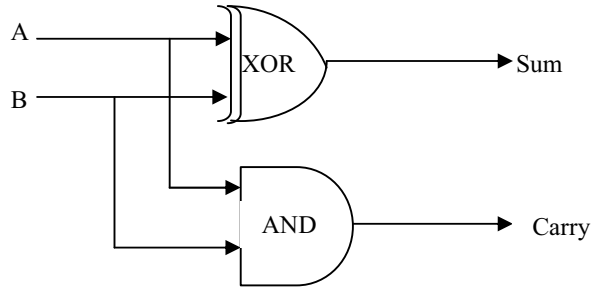

Fig.2. Logic gate symbol of half adder

The Boolean functions for the outputs can be obtained by truth table. The simplified sum of products expressions are

SUM = A'B+AB' (1)
CARRY = A.B (2)

TABLE.I TRUTH TABLE OF HALF ADDER:

Input		Output	
A	***B***	***Sum***	***Carry***
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

A. Logic gate description for implementation of half adders

1) XOR gate: The XOR gate (Exclusive or, EX-OR) gives HIGH output (1) results if only one, of the inputs to the gate is HIGH (1). If both inputs are LOW (0) and both are HIGH (1), a LOW output (0) results. A simple way to consider that XOR gate represents the output is HIGH (1) if the inputs are different otherwise the output is LOW (0).

The XOR logic gate can be used as adder that adds any two bits together to output one bit. If we add 1 plus 1 in binary, we expect a two bit answer, 10 (i.e. 2 in decimal). By XOR the output sum bit is achieved, the carry bit is calculated with the help of AND gate. In order to add longer binary numbers half adder is combined with XOR-AND circuit may be chained together [7]. This gate is designed by using twelve transistors in which six are PMOS and six are NMOS transistor. The pull-up network (PMOS) is connected to power supply (VDD) and pull down network (NMOS) connected to ground (VSS). In the schematic of XOR gate, left and right side inverter represents the complement inputs (A' and B'). XOR gate is fundamental building block of full adders, enhancing the performance significantly and improve the performance of the adders [9].

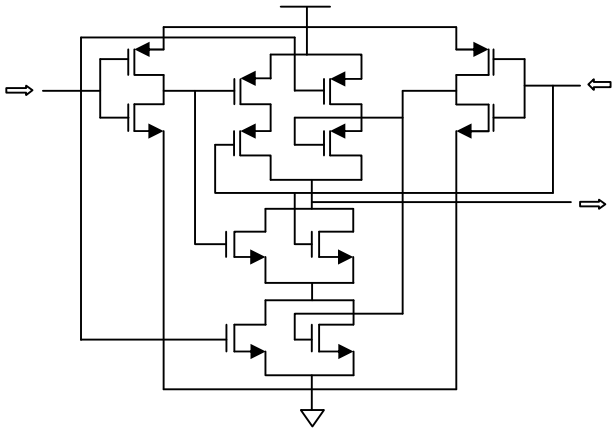

Fig.3. Transistor level schematic of XOR gate

Expression of XOR gate is:

Z = A'B+AB' (3)

TABLE.II TRUTH TABLE OF XOR GATE:

Input		Output
A	***B***	***Z***
0	0	0
0	1	1
1	0	1
1	1	0

2) AND gate- The AND gate is a basic digital logic gate that perform logical conjunction, that is, a HIGH output (1) results only if both the inputs to the AND gate are HIGH (1). If neither or only one input to the AND gate is HIGH (1), a LOW

(0) results. The output is always low (0) except when all the inputs are HIGH (1). The AND gate function finds the minimum between two binary digits, just as the OR function finds the maximum.

Expression of AND gate is

$$AND=A.B \quad (4)$$

TABLE.III TRUTH TABLE OF AND GATE IS:

Input A	Input B	Output Y
0	0	0
0	1	0
1	0	0
1	1	1

The AND gate schematic consist of six transistor in which three PMOS transistors are connected to pull-up (VDD) network and three NMOS transistors are connected to pull down (VSS) network. The purpose of pull up network is when the output of logic gate is at high logic it provide a connection between the output and VDD [5].

LEAKAGE CURRENT AND LEAKAGE POWER

Sometimes few functional blocks or whole circuit is not in use, it must be quickly deactivated, so that it consumes almost no power. Still leakage current flows in idle mode causing some power consumption. Therefore a key to a low power design is to incorporate the techniques to diminish leakage power. The circuit level techniques are further classified into static and dynamic techniques. The static techniques include design optimization methods and circuit styles. Dynamic techniques can be applied at many levels of designing steps and these techniques put the design in low leakage mode when the design enters into a standby condition.

Leakage current is a major effective factor in CMOS circuit which reduces the performance of the device. As thickness of insulating region in CMOS is decreases the leakage is increases also. In this technology leakage occurs at gate insulator junction, carriers can also leaks between source and drain terminals. Three major components of leakage current are junction tunneling current, sub-threshold current, and gate tunneling current. Standby leakage power also increases with increasing silicon technology. The expression for power calculation is [4].

$$P = \frac{1}{t} \int i \, dt \quad (5)$$

Where P = leakage power
t = time period
I = leakage current
V = supply voltage

In nanometer regime, standby leakage power becoming important parameter of the circuit performance. Leakage in standby mode is larger than active mode. This needs the low power design using scale down the supply voltage. The stand-by power consumption is accounted by the 3rd term. The dynamic power consumption is reduces by Using a lower VDD supply [29]. Total power includes static and dynamic component which is expressed during the active mode of operation as

$$P_t = P_{static} + P_{dynamic} + P_{short\ circuit} \quad (6)$$

$$= V_{DD} I_i + V_{DD} f_{clk} \sum V_{iswing} C_{iload} \alpha_i + V_{DD} \sum I_{isc} \quad (7)$$

Where f_{clk} = system clock frequency
V_{iswing} = voltage swing at node i
C_{iload} = load Capacitance at node i
α_i = activity factor
I_{isc} = short circuit current

In the sub threshold region, the device threshold voltage is higher than power supply voltage. This confirms that the transistor channel is never fully inverted, but is accomplished in weak or moderate inversion while the transistor is in its 'on' state. Due to the exponential V-I relationship, sub-threshold logic gates have a near ideal voltage transfer characteristics [10].

Expression (6) is also expressed as $P = ACV^2f + V_{leak}$ (8)

Where A = fraction of gates actively switching and
C = total capacitance load of all gates
I_{leak} = static power lost due to leakage current

As we know the power dissipation in digital circuits has three components active, leakage and short circuit leakage. Power dissipation is controlled by the switching and leakage component. The short circuit leakage power is proportional to switching power of circuit. That is equal to the rate of energy and also product of switching energy and frequency of operation.

$$P_{sw} = E_{swf} = \alpha \, C \, VDD^2 \, f \quad (9)$$

Where E_{sw} = switching energy
C = total capacitance
α = switching activity
f = operating frequency

.

$$P_{leak} = VDD * I_{leak} \quad (10)$$

Here leakage power is product of supply voltage and leakage current 'I_{leak}'. With reduction in threshold voltage sub threshold leakage current increases exponentially. This is critical for low voltage circuit design [11]. In sub 100nm technology the leakage power is expected to reach more than 50% of total power [14]. The increasing scaling of device dimensions and threshold voltage has significantly increased the gate and sub-threshold leakage currents exponentially, and within earlier process it is predicted that dynamic switching energy could be comparable to energy dissipations from static leakage currents [15].

In low power designs it is a usual approach when parts of the circuit are not in use put the circuit in 'standby' mode by holding the clock fixed to reduce dynamic power dissipation.

When place the circuit in a static standby state it exhibits low gate leakage. A large circuit makes with specific logic gates to produces a small total leakage current we must search for an input vector that, which can be computed using state-dependent leakage tables. During an idle period minimum additional circuitry large multi-gate circuit and sub-threshold leakage methodology finding a low leakage state [10].

The basic half adder has a complex structure that affects the overall complexity of a computer's structure. Advanced DNA computing has gained accurately realizes computations and overcomes the shortcomings of traditional integrated circuit half adders, optical half adders, and chemical molecule half adders, such as complex structure, limited component size, and low accuracy [16].

With increasing the W/L ratios of all transistors in the circuit we increase the switching speed, and reduce the delay time. However, increase in this ratio also increases the gate, source, and drains areas as a result, increases the parasitic capacitances loading to the logic gates [17].

In digital circuits the propagation delay, or gate delay, is the time duration which starts when the input to a logic gate becomes stable and valid to change, to the time that the output of that logic gate is stable and valid to change. The time required for the output to reach 50% of its final output level when the input changes to 50% of its final input level. In digital circuits reduced gate delays allows the process data at a faster rate and improve overall performance.

Scaling is also important to minimize power consumption. Supply voltage always scaled along with the threshold voltage so as to minimize the propagation delay which is an imparting and most controllable significant factor. This sub-threshold scaling causes to an increase in leakage current. This results to dissipation of power in the digital circuits, when resided in sleep or standby mode [22].

Battery operated wireless communication has generally consumes the largest sum of power in a wireless front end it admired for many applications to reduce the battery size, area, delay, power and channel selection, so it needs to be compact [23, 24].

I. HALF ADDER WITH SELF-VOLTAGE CONTROLLABLE (SVL) LOGIC

SVL is combination of L-SVL and U-SVL [8],When the half adder circuit is in active mode (i.e. upper sleep-bar signal is low (0) and lower sleep signal is high (1)), both p-SW and n-SW are in ON state or working state, on other hand nRS1and pRS1 are in OFF state, therefore, the U-SVL and L-SVL circuits supply the maximum voltage VDD (i.e. 0.7v at 45 nm technology) and a minimum ground state voltage (VSS = 0v) respectively to the active load circuit, therefore the operating speed of the half adder circuit can be maximized. While the half adder is in off state (i.e. upper sleep-bar signal is high (1) and lower sleep signal is low (0)), all p-SW and n-SW are in off state or standby mode, so the U-SVL and L-SVL circuit respectively generates a minimum supply voltage Vdd and a relatively higher ground level voltage VSS, therefore, leakage currents or stand by current of the cut off MOSFETs decrease.

In active mode of operation, logic circuit gets connected to the VDD and ground lines through 'on' SVL transistor switches causing the usual operation. In standby mode of operation, the logic circuit gets disconnected through the 'off' SVL switch transistors [18-19]. In this mode, it supplies low voltage through the weakly-on switches [27]. SVL provides better leakage power reduction with minimal area overhead in multipliers [20] and that not only reduces leakage power but also retains data during stand by period [21]. We evaluate the performance of the SVL techniques in terms of leakage current and leakage power. A 1-bit half adder circuit implemented with cadence virtuoso tool. Leakage reduction techniques are then implemented over this standard 18-transistors half adder. It can be concluded from the simulation results shown in the table that SVL scheme provides efficient leakage power saving, with improved leakage power reduction capability. Adders have advantage in field of Power-delay product (PDP), speed and area with micrometer regime [26].

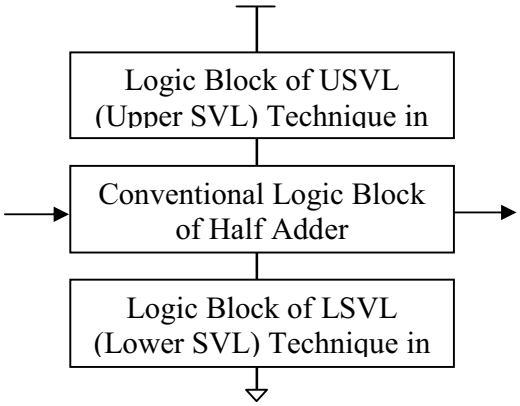

Fig.5. SVL Technique implementation in half adder

Leakage power reduction techniques can be grouped into two categories. In state preserving techniques; the circuit retained the state and in state-destructive techniques; the current Boolean output value of the circuit might be lost [28].

Advantage of state-preserving technique over a state destructive technique is that in this circuitry can resume operation at a point much later in time without having to somehow regenerate state. Half Adder is very useful in digital arithmetic circuits for state preserving technique.

SIMULATION RESULTS

The half adder is a combinational circuit that analyzes the addition of two input bits. In the simulation table total power, signal to noise ratio (SNR), leakage current and leakage power are find out. All these parameters of conventional half adder and SVL (both USVL and LSVL) shown in the table. We simulate the circuit of half adder at 0.7 volt supply voltage using cadence virtuoso simulation tool in 45 nm technology. By using the SVL technique leakage current and leakage power is reduced as compared to conventional CMOS half adder circuit.

TABLE.IV SIMULATION RESULT OF HALF ADDER AT 45 NANOMETER TECHNOLOGY

Parameters (at 45 nm Technology)	Conventional CMOS Half Adder	Half Adder with SVL (Active mode)	Half Adder with SVL (Stand-by mode)
Total power (nW)	40.19	38.0	1.295
SNR (db)	2.042	1.985	0.347
Leakage current (pA)	2.407	2.462	1.691
Leakage power (pW)	1.955	2.156	2.611

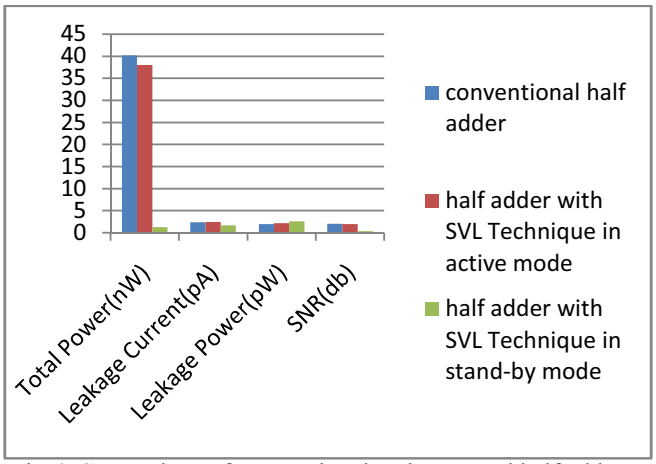

Fig.6. Comparison of conventional and proposed half adder

VI.CONCLUSION

In this paper we proposed the half adder combinational circuit with SVL technique which performs the addition of two bits with low leakage power. SVL technique is better effective than conventional half adder by providing low power design methodologies. This technique has single threshold implementation controls the leakage current by disconnecting the supply to inactive block and maintains the performance by low leakage current in sleep mode. Simulation result shows that SVL technique reduces the total power, leakage current and signal to noise ratio (SNR) as compared to conventional CMOS half adder in standby mode at 45 nm Technology.

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