High Performance CMOS Current Comparator using MTCMOS Technique Design

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***Abstract*— This paper presented a simulation result of current comparator with low power and low leakage current using Multi-Threshold CMOS technique (MTCMOS). In all integrated circuit power consumption plays a vital role which is enumerated as top challenges for semiconductor in international technology .In given paper designing a circuit of comparator with MTCMOS circuit and without MTCMOS circuit and then compared these circuits with different parameters by changing voltage, frequency and temperature. In these CMOS current comparator circuit different parameters calculated like delay, power dissipation, signal to noise ratio, leakage power and leakage current. The multi-threshold complementary metal oxide semiconductor technique is proposed to reduce the power consumption and leakage current. After propagating the circuit the leakage power is reduced 89% and leakage current 73% using MTCMOS technique. The new comparator has been in 180nm technology using cadence tool. The simulation and analytical result show that the proposed circuit is correct.**

***KEYWORDS*- PROPAGATION DELAY, SPEED, POWER DISSIPATION, CURRENT COMPARATOR, LOW LEAKAGE, MTCMOS**

I. INTRODUCTION

The comparators are most widely used as electronic parts. Current comparators have essential building blocks in several analogue circuits designing, mainly in support of front-end signal dispensation application and increase inside Neuro-morphic electronic system [1]. The SRAM has been depending on two standby mode one is resume standby mode to reduce the standby current at room temperature and second is conventional resume standby mode for reducing effectively at high temperature [2]. A single variable and resistive ratio winding are utilized to achieving excellent dynamic stability for low current [3]. A latch type comparator design will be focusing on minimization of propagation delay and the power consumption [4]. A new type of comparator design for high performance and low input current by adding two inverters in feedback loop [5]. The comparator architecture divided into two stages first is novel tree structure designing for static logic for low power consumption and second is logic utilized cd logicfor high performance without energy efficiency [6]. As down-scaling of CMOS process the analog circuit has been strained to activate with constantly decrease the supply voltage [7]. This method has been broadly funded by reducing power supply consumption inside mixed-mode VLSI system. The signal attributes of a current mode approach for example large bandwidth, high speed and decrease have to high supply voltage etc. which have made the analogue designer for taking the extra attention in the current mode circuit.

This is essential that comparators have high speed when these are distributed diagonally in a processing display with low power and the propagation delay working about 10ns. In the preceding days, typically use the voltage comparator which coincidence various enormous difficulty like power consumption, operational frequency and input offset voltage. The current correlation has been arranged by influence the current pulse in the input node of comparator with high speed and low leakage [8]. The analog to digital converters are commonly scheduled for lots of applications like high speed measurement system fast. Serial link and data storage system, in such analog to digital converter comparators are playing an essential role with more accuracy and speed [9].

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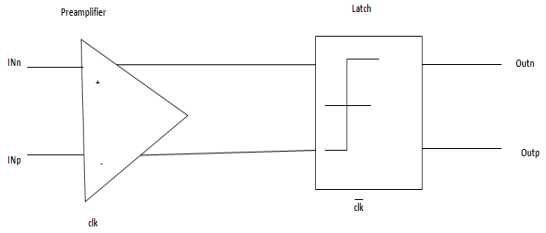

Figure1. Block Diagram of Comparator [18]

The output of comparator circuit is supplied by comparing the input waveforms. In this mode the comparator containing the current signal which implements by a current mode technique which occupies low power dissipation, small area and high speed. A comparator circuit is applied to provide output for indicating the termination of cognitive process [8].The new circuit of the comparator is restricted by the necessity of lowest input current 10pA for performing the operation which granted slanted output signal under this value.

Many techniques have been suggested to minimize leakage power in digital circuits. Here we use MTCMOS (Multi Threshold Complementary metal Oxide Semiconductor) technique for designing a high speed, low leakage power efficient half adder in 180 nanometer technology. MTCMOS technique effectively used to build logic circuits with high speed and small power dissipation as compared to traditional

CMOS. MTCMOS is circuit level technique that improves the performance and provides low power circuit by using both low and high threshold voltage transistors [10]. D. forts' and K. current [11] firstly proposes a new set of comparator called a current comparator. He gave a complementary metal oxide circuit of current comparator for high performance. Chung-Yu Wu, Chih-cheng chen,Ming-kai Tsai and Chih-Che Cho[12] Designing current comparator schematic without offset at which minimum current containing 0.5μA.

The Main disadvantage of this comparator is that it requires many transistors and more power dissipates. H.Traff [13] giving a humble and high speed current comparator. This conventional comparator uses a CMOS inverter as positive feedback and a source follower as input, but the output punching could not reach to the power supply. In this circuit the operation is restricted by the lowest value of input current is 10nA, below this value provided distorted output signal. G. Palmisano and G. Palumbo [14] proposed a comparator with offset compensation of offset current due to the process of mismatching of the transistor. In this circuit the capacitor employed to reduce the operating speed but drawback is that this increase manufacturing. But one drawback of this circuit is that speed is very less when compare by proposing circuit. G.Palisano and S.Pennisi [15] gave a novel technique for comparator with the current amplifier circuit in which response time containing 50ns for 5μA, which showing more value delay as compared with recently published paper.

In presenting paper we are comparing the result of MTCMOS based comparator circuit and CMOS based comparator circuit [16].

II.IMPLEMENTATION OF CURRENT COMPARATOR USING CMOS TECHNOLOGY

In CMOS (Complementary metal oxide semiconductor configuration) designing a circuit with complementary push - draw on the logic that we have both PMOS and NMOS networks are incorporated in the circuit. Accordingly both devices supply equal to the circuit processing characteristic. There are mainly three sources of power dissipation in digital CMOS circuit [17].Finally, leakage current arises from sub-threshold effects and substrate injection.

III.SCHEMATIC REPRESENTATION OF CURRENT COMPARATOR USING CMOS TECHNOLOGY

In Figure 2 Showing the circuit diagram of conventional current comparator. In this the circuit consisting 5- part such as a standard current mirror, input current pulse generator, Wilson current mirror, CMOS inverter and power supply. Wilson current mirror mainly used for reducing the total power dissipation. In this current comparator circuit uses high output impedance of current mirror for amplifying the differences of input current for large variation in output voltage. Then simulating the result transient response and DC response of the circuit performed [18] if input current given ±10Pa.

The transient analysis of input signals varies from 1mA to 10pA. The comparator works successfully till 10pA below this value output starts distorted. The comparators are given approx constant value by changing the input current of the circuit. The DC analysis has been performed for computing the full ability of new current comparator. The power consumption of circuit giving in condition of input current ± 400pA then the average power is consumes 4.061nW.

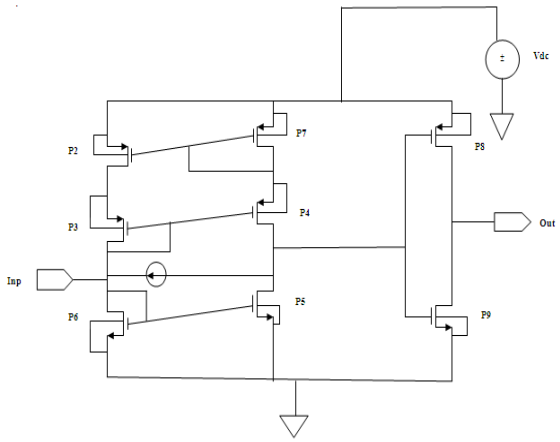

Figure 2. A transistor level schematic of Current Comparator

IV.IMPLEMENTATION OF CURRENT COMPARATOR USING MTCMOS TECHNIQUE

The supply and threshold voltages are reduced by scaling of CMOS technology. By lowering of threshold voltage load an exponential increase in the sub threshold leakage current [13]. In recent high performing integrated circuits (ICs) are more than 22% of the total energy can be dissipated due to leakage current. With additional transistor integrated ICs, leakage current will soon control the total energy consumption with high performed ICs. A popular low leakage circuit technique is known as Multithreshold Voltage CMOS (MTCMOS).

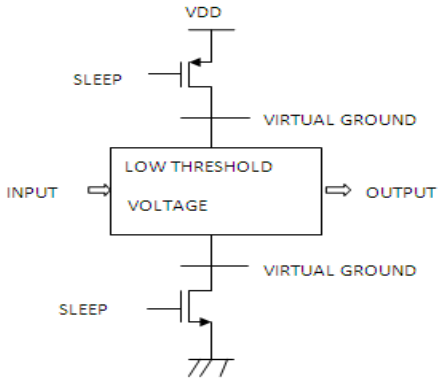

Figure 3: MTCMOS technique using sleep transistors

The multi threshold CMOS technology has two main features. The First is "active" and other is "sleep". In this technique the operational modes are linked with MTCMOS technology with efficient power managing. Second thing two

different threshold voltages are used for N channel and P channel MOSFET in a single chip [15]. This technique based on disconnecting the lower threshold voltage (low-Vt) logic gates from the power supply and the ground line via cutoff high threshold voltage (high-Vt) sleep transistors is also known as "power gating".

The schematic of power gating technique using MTCMOS is shown in Fig.3.The transistors having low threshold voltage which is used to implement the logic. In the active mode, sleep transistors are turned on and the logic consisting of low VT (threshold voltage) transistors can operate with high speed and low switching power dissipation. When the circuit is in sleep mode the high VT transistors are turned off causing isolation of low VT transistor from supply voltage and ground thereby reducing sub-threshold leakage current.

The transistors having high threshold voltage are applied to set apart the low threshold voltage transistors from supply and ground during standby (sleep) mode to prevent leakage dissipation [16].

V.LEAKAGE CURRENT AND LEAKAGE POWER

The leakage current is the most important factor of CMOS circuit which reduces the performance of any circuit. In CMOS technique leakage occurs due to gate insulators and junction, by which carriers can also leak between drain and source terminal. There are mainly three components of leakage current: sub-threshold current, gate tunneling current and junction tunneling current.

By increasing order of scaling the threshold voltage and device dimension has extensively increased the gate and sub-threshold leakage and within some process it is predicted energy consumptions from static leakage currents to dynamic energy [19]. By reason of more power dissipation the MTCMOS technique reduces leakage up to 2-3 order of magnitude which is depending on size of sleep transistor and threshold voltage, for a moment the addition of sleep transistor causes an increase in delay of the circuit.

In the CMOS technique the entire power consumption of the circuit is a combination of static power and dynamic power during on mode. This circuit needs the low power designing by using of scale down the supply voltage. For a CMOS circuit total power PT includes static and dynamic component during the active mode operation. It can be expressed as

$$PT = Pstatic + Pdynamic \quad (1)$$

The static power for CMOS circuit is defined as the leakage current in each transistor. On the other hand the dynamic power consists of dual mechanism first is switched power by charging and discharging of system and second is short circuit power by imperfect fall time and rise time of the input waveform [23]. Then leakage power P_{LEAK} is shown as

$$P_{LEAK} = Vdd\, I_{LEAK} \quad (2)$$

Sub threshold leakage current exponentially increases with reduction of threshold voltage.The leakage current [20] is calculated from equation 3. at the time when the transistor is in the off condition.

$$I_{sub} = \mu_0\, C_{ox} \frac{W}{Leff} V_T^2\, e^{1.8}\, \exp\left(\frac{Vgs-Vth}{nVT}\right).(1 - \exp\left(-\frac{V_{ds}}{V_T}\right)) \quad (3)$$

The average power consumption of the circuit requires some input vector to obtain accurate estimation. Then average power [22] at interval time is shown as

$$P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T i_{DD}(t).V_{DD}\,dt \quad (4)$$

If P(t) is the instantaneous power which is proportional to the supply voltage V_DD [22] and supply current i(t) is shown as

$$P(t)=i(t).Vdd \quad (5)$$

Table I. shows the comparison of leakage current and leakage power between current comparators. We simulate the circuit of comparator using the cadence simulation tool in 180 nanometer technology. At this time we have been using the proposed MTCMOS technique that reduces the leakage current and leakage power of current comparator circuit when compared to CMOS technique. With the help of this technique leakage current is reduced by 73% and leakage power is reduced by 89%.

TABLE I. COMPARISON OF LEAKAGE CURRENT AND LEAKAGE POWER BETWEEN CURRENT COMPARATORS

Current Comparator	MTCMOS based Current Comparator	CMOS Based Current Comparator	% Reduction
Leakage Current(pA)	1.429	5.259	73%
Leakage Power(pA)	4.597	39.26	89%

TABLE II. COMPARISON OF PROPAGATION DELAY BETWEEN CURRENT COMPARATORS

Input Current	Propagation delay in nano-sec.	
	CMOS technique based current comparator	MTCMOS technique based current comparator
1 mA	20.73	19.02
100 µA	20.60	19.13
10 µA	20.54	19.17
1 µA	20.53	19.18
400 nA	20.53	19.18
100nA	20.53	19.21
10nA	20.53	19.30
400pA	20.53	19.28

In table II when contrast proposed comparator to conventional comparator then the new comparator circuit is operates with high speed.

Figure 4. shows the delay time versus input current graph As shown in the graph we are comparing the propagation delay of

proposed comparator are less than to the propagation delay of conventional comparator.

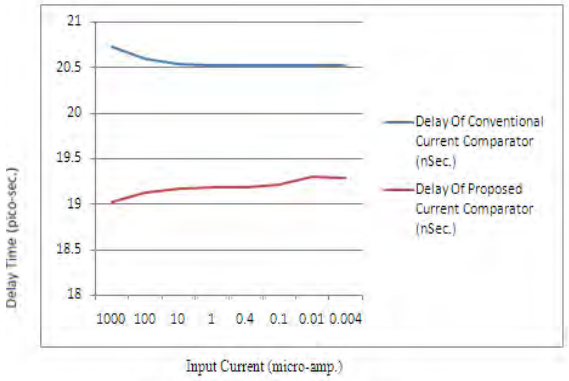

Figure 4. Delay Time versus Input Current

In following table III shows the power consumption between the conventional current comparator (CMOS based) and proposed current comparator (MTCMOS based) after simulating the circuit. After simulating the results we observe that the power dissipation of new comparator is much lesser than to conventional comparator.

TABLE III. COMPARISON OF POWER DISSIPATION BETWEEN CURRENT COMPARATORS

Input Current	Power dissipation in µW	
	CMOS technique based current comparator	MTCMOS technique based current comparator
1 mA	979.1	756.7
100 µA	848.1	31.55
10 µA	847.5	2.220
1 µA	847.4	0.183
400 nA	847.3	0.071
100nA	847.3	0.020
10nA	847.3	0.006
400pA	847.3	0.004

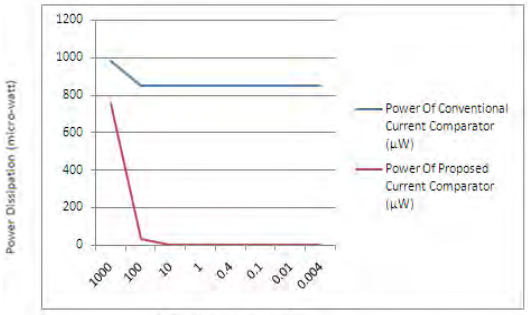

Figure 5. Power Dissipation versus Input Current

Figure.5. Shows the power consumption versus input current graph. As shown in the graph we are comparing the power of proposed comparator is less than two powers consumed by conventional comparator.

In following table IV shows the signal to noise ratio of the conventional current comparator (CMOS based) and proposed current comparator (MTCMOS based) after simulating the circuit.

TABLE IV.COMPARISON OF SIGNAL TO NOISE RATIO BETWEEN CURRENT COMPARATORS

Input Current	Signal to noise ratio in dB	
	CMOS technique based current comparator	MTCMOS technique based current comparator
1 mA	0.780	2.449
100 µA	0.717	0.538
10 µA	0.676	0.417
1 µA	0.156	0.384
400 nA	0.155	0.354
100nA	0.155	7.281
10nA	0.155	8.972
400pA	0.674	10.514

Figure 6. shows the signal to noise ratio versus input current graph. As shown in the graph we are comparing signal to noise ratio of proposed comparator is greater than the signal to noise ratio of conventional comparator.

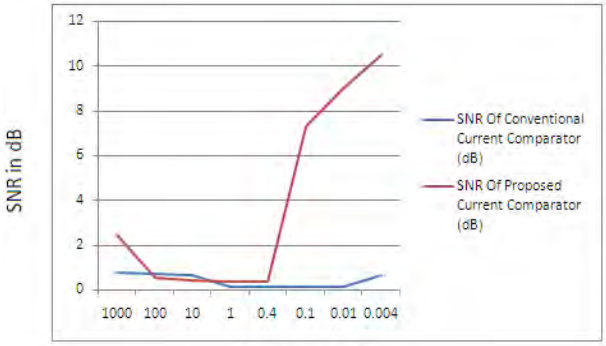

Figure 6. Signal to noise ratio versus input current

VI.CONCLUSION

In this paper we proposed a current comparator circuit which compares the conflict between two signals and given a specified value. The Proposed MTCMOS technique is better effectively reduces the leakage current and leakage power of current comparator. For reducing the leakage current and leakage power enhanced a new circuit with double sleep transistors called the MTCMOS based current comparator. This provides low design methodologies by using low as well as high threshold voltage transistors. Simulation result shows that this technique reduces the leakage current by 73% and leakage power by 89%.The Simulation and results for a current

comparator is done by the Cadence virtuoso tool in 180 CMOS nanometer technology at various supply voltages and current.

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REFRENCES

[1] D.Banks, and C.Toumazou, "Low-Power high-speed current comparator design", IEEE Proceedings –Electronics Letters, vol.44, no.3, pp. 171-172, January 2008.

[2] Moeda N., komatsu,S.; Monmoto M.,Tanaka K., Tsukamoto Y., Nii K.., shimazaki Y., " A 0.41µA standby leakage 32kb embedded SRAM with low voltage resume-standby utilizing all digital current comparator in 28nm HKMG CMOS", IEEE journal of solid – state circuits, vol.48, no.4, pp. 917-923, January 2013.

[3] Hernandez. Marquez F. L., Bierzychudek M.E., Jones G.R., Elmquist R.E., " Precision high-value resistance scaling with a two terminal cryogenic current comparator", IEEE review of scientific instruments, vol.85, no.4, pp. 044701-044701-6, April 2014.

[4] Halim I.S.A., Abidin N.A.N.B.Z., Rahim A.A.A., " Low power CMOS charge sharing dynamic latch comparator using 0.18µm technology, IEEE regional symposium on micro and nanoelectronics (RSM), pp. 156 – 160, September 2011, Kota kinabalu, India.

[5] Tang X.,Pun K.-P. , " High performance CMOS current comparator" IEEE proceeding – electronics letters, vol.45, no.20, pp. 1007 – 1009, September 2009.

[6] Chuang, P.I.-I, Sachdev M., Gaudet V.C., " A 167-ps 2.34-mW single-cycle 64- bit binary tree comparator with constant delay logic in 65-nm CMOS" IEEE transactions on circuit and systems, vol.61, no.1, pp. 160 – 171, January 2014.

[7] Carvajal R.G., Ramire- Angulo J., Lopez-Martin A.J., Torralba A., Galan J.A.G., Carlosena A. and Chavero F.M., "The flipped voltage follower: a useful cell for low – voltage low – power circuit design", IEEE transaction on circuit and systems I, vol.52, no.7, pp.1276-1291, July 2005.

[8] Vinai Thrivikramaru, Rajendra Kumar Baghel, "High Speed Average Power CMOS Current Comparator", proceeding of IEEE International Conference on Communication Systems and Network Technologies, pp.745-749, May 2012, Rajkot, India.

[9] Samaneh Babayan- Mashhadi, Reza Lotfi, "Analysis and Design of a Low-Voltage Low Power Double-Tail Comparator", IEEE Transaction on Very Large Scale Integration Systems, vol.22, no.2, pp.343-352, February 2014.

[10] H. Traff, "Novel Approach to High Speed CMOS Current Comparators", IEEE Proceeding – Electronic Letters, vol.28, no.3,pp. 310-312 , January 1992.

[11] D. Freitas and K. Current, "CMOS Current Comparator Circuit", IEEE Proceeding- Electronics Letters, vol.19, no. 17, pp. 695-697, August 1983.

[12] Chung- Yu Wu, Chih- cheng chen, Ming-kai Tsai and Chih-Che Cho, "A 0.5µA Offset- Free Current Comparator For High Precision Current-Mode Signal Processing", IEEE International Symposium on Circuits and Systems, vol.3, pp. 1829-1832, June 1991.

[13] G. Palmisano and G. Palumbo, "High Performance CMOS Current Comparator Design", IEEE Transactions on Circuits and Systems, vol.43, no.12, pp.785- 790, December 1996.

[14] G.Palmisano and S.Pennisi, "Dynamic Biasing for True Low-Voltage CMOS Class AB Current-Mode Circuits", IEEE Transaction on Circuits and System-II: Analog and Digital Signal Processing, vol.47, no.12, pp.1569-1575, December 2000.

[15] Shyam Akashe, Jayram Shrives, Nitesh Tiwari, Rajeev Sharma, "A Novel High Speed and Power Efficient Half Adder Design Using MTCMOS Technique in 45 Nanometre Regime" proceeding IEEE International Conference on Advanced Communication Control and Computing Technologies (ICACCCT), Ramanathapuram, August 2012.

[16] A.P. Chandrakasan, S. Sheng and R. W. Brodersen, "Low power CMOS digital design" IEEE journal of solid and state, vo.27, no.4, pp.473-484, April 1992.

[17] Borivoje Nikolic, "Design in the Power-Limited Scaling Regime", IEEE Transaction on Electron Devices, Vol.55, No.1, January 2008.

[18] F. Fallah, M. Pedram, "Standby and Active Leakage Current Control and Minimization in CMOS VLSI Circuits", IEICE Transactions on Electronics, pp.509-519, Vol.E88- C(4),2005.

[19] Shyam Akashe and Sanjay Sharma, "High density and Low Leakage Current Based SRAM all using 45nm technology", proceeding of IEEE International Conference on, pp.346-350, November-2011, Chennai, India.

[20] Akansha Shrivastava, Saurabh Khandelwal and Shyam Akashe, " Low Power Analysis in Single Stage Source Coupled VCO with AVL technique using nanoscale CMOS Technology", IEEE Conference on Emerging and Systems, pp. 1-6, April 2013, Allahabad, India.

[21] Upendra Soni, Abhay Vidyarthi and Shyam Akashe, "Design of High Speed and Leakage Tolerant CMOS Comparator in UDSM Technologies", IEEE Third International Conference on Advance Computing and Communication Technologies, pp. 326-329, April 2013, Rohtak ,India .

[22] Byung-moo Min and Soo-won Kim, "High performance CMOS current comparator using resistive feedback network", IEEE Proceeding-Electronic Letters, vol.34, no.22, pp. 2074-2076, October 1998.

[23] Shabi Tabassum, Anush Bekal, Manish Goswami, "A Low Power Preamplifier Latch Based Comparator Using 180nm Technology", IEEE Asia Pacific Conference on Postgraduate research in microelectronics and electronics, pp. 208-212, December 2013, Visakhapatnam, India.

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