International Conference on Innovative Applications of Computational Intelligence on Power, Energy and Controls with their Impact on Humanity (CIPECH14) 28 & 29 November 2014

A PFC Based Bridgeless Sheppard-Taylor Converter fed Brushless DC Motor Drive

Vashist Bist, *Student Member, IEEE*
Department of Electrical Engineering,
Indian institute of Technology Delhi,
Hauz Khas, New Delhi-110016.
e-mail: vashist.bist@gmail.com

Bhim Singh, *Fellow, IEEE*
Department of Electrical Engineering,
Indian institute of Technology Delhi,
Hauz Khas, New Delhi-110016.
e-mail: bsingh@ee.iitd.ac.in

***Abstract* — A power factor correction (PFC) based bridgeless Sheppard-Taylor converter for feeding brushless DC (BLDC) motor dive is presented in this work. The voltage of DC bus of the voltage source inverter (VSI) feeding BLDC motor is adjusted for speed control. The BLDC motor is electronically commutated to operate the VSI in low switching frequency for reducing the switching losses in it. The proposed PFC converter is operated in discontinuous inductor current mode (DICM) for inherent power factor correction using a single voltage sensor. The performance of the proposed PFC converter feeding BLDC motor drive is evaluated for control of speed over a wide range. A unity power factor is achieved with power quality indices acceptable within the limits of IEC 61000-3-2.**

***Keywords*—Brushless DC motor, bridgeless Sheppard-Taylor converter, power factor correction, power quality, voltage source inverter.**

I. INTRODUCTION

Brushless DC (BLDC) motors are highly efficient motors and possess high power-density, high ruggedness, high torque/inertia ratio and silent operation [1, 2]. These motors find applications in household equipments, industrial tools and precise motion control systems. This motor is a three phase synchronous motor with three-phase concentrated winding on the stator and permanent magnet on the rotor [1, 2]. The rotor position of BLDC motor is sensed by Hall Effect position sensors for the commutation of the BLDC motor, electronically. This electronic commutation is based on switching table in which six switches of voltage source inverter (VSI) feeding BLDC motor are turned on and off depending upon the current rotor position [2].

In a conventional scheme of BLDC motor drive, a diode bridge rectifier (DBR) and a DC link capacitor are used for feeding BLDC motor; which draws highly distorted supply current from the AC mains [3]. Such current has high amount of harmonics and results in high total harmonic distortion (THD) of supply current of the order of 60-80 % which results in power factor as low as 0.65 and crest factor (CF) as high as 3-5 [3]. Such indices are not under acceptable under the limits of international standard such as IEC 61000-3-2 [4]. Hence, single-phase power factor correction (PFC) converters are used for achieving a unity power factor at AC mains [5, 6].

These PFC converters are generally designed for its operation in continuous or discontinuous conduction modes. In continuous conduction mode (CCM), sensing of the supply voltage, the DC bus voltage and the input current is required to achieve voltage control with PFC operation [6]. This offers an advantage of reduced stress on the switch of the PFC converter. However, it requires high amount of sensing and preferred in medium and high power applications. Moreover, sensing of single DC link voltage is required for a PFC converter operating in discontinuous conduction mode (DCM). However, the stresses on PFC converter switch increases in this mode and therefore used in low power applications [6].

A BLDC motor drive fed by a PFC boost converter has been the most widely used configuration [7]. A constant DC bus voltage is maintained at the DC bus capacitor and the speed is controlled by varying the duty-ratio of pulse width modulation (PWM) signals given to VSI. Such high switching frequency causes high switching losses in the six switches of VSI which reduces the overall efficiency of the system. These losses are reduced by commutating the BLDC electronically, which requires low frequency switching of VSI [8-11]. Moreover, the speed of BLDC motor is adjusted by varying the DC bus voltage of the VSI feeding BLDC motor. Hence, buck-boost PFC converters are used for these applications due to voltage control over a wide range at varying supply voltages [8-11].

Bridgeless PFC converters are designed for reducing the losses associated at the front-end converter by complete or partial elimination of the DBR. Moreover, a Sheppard-Taylor converter receives wide attention due to its ability of good voltage regulation, high light load efficiency and no control-detuning problems (inability of PFC converter to shape supply current at zero crossings) [12-14]. Incorporating the advantageous features of this PFC converter, a new bridgeless configuration of a Sheppard-Taylor converter fed BLDC motor drive is presented in this paper as shown in Fig. 1. The proposed PFC converter is designed in dual DCM, such that the input (L_{i1} and L_{i2}) and output (L_{o1} and L_{o2}) inductors operate in discontinuous conduction. Moreover, the BLDC motor is electronically commutated, which in-turn reduces its switching losses. An improved performance in terms of unity power factor and low supply current THD of the proposed drive for speed control over a wide range is evaluated in this work.

©2014 CIPECH14.

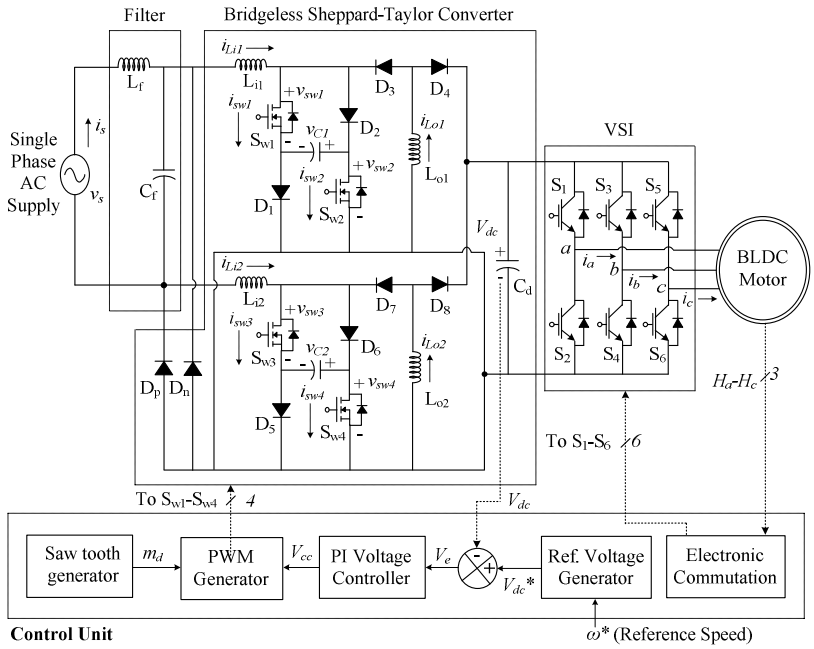


Fig. 1. Proposed configuration of a PFC based bridgeless Sheppard-Taylor converter feeding BLDC motor drive.

II. Operation of Proposed PFC Converter

The operation of proposed PFC based bridgeless Sheppard-Taylor converter is classified into two parts as follows.

A. Operation during Two Half Cycles of Supply Voltage

The bridgeless converter is designed such that two different switches operate in two half cycle of supply voltage. As shown in Figs. 2 (a-d), switches (S_{w1}, S_{w2}), inductors (L_{i1}, L_{o1}), intermediate capacitor (C_1) and diodes (D_p, D_1-D_4) conduct during the supply voltage's positive half cycle and vice versa for negative half cycle of supply voltage.

B. Operation during Complete Switching Cycle

Figs. 2 (a-d) show four operating modes of proposed PFC converter during a switching period and Fig. 2 (e) shows the associated waveforms.

Mode I: When switches S_{w1} and S_{w2} are conducting, then input inductor L_{i1} and output inductor L_{o1} start charging as shown in Fig. 2 (a). However, the intermediate capacitor (C_1) and DC link capacitor (C_d) start discharging as shown in Fig. 2 (e).

Mode II: When switches S_{w1} and S_{w2} are turned off, both inductors (L_{i1} and L_{o1}) start discharging as shown in Fig. 2 (b). Whereas the intermediate capacitor (C_1) and DC link capacitor (C_d) start charging as shown in Fig. 2 (e).

Mode III: In this mode, input inductor (L_{i1}) is completely discharged and enters DCM mode as shown in Fig. 2 (c). The output inductor (L_{o1}) continues to discharge in this mode, as shown in Fig. 2 (e).

Mode III: In this mode, both inductors (L_{i1} *and* L_{o1}) are completely discharged and enters DCM mode as shown in Fig. 2 (d). The DC link capacitor supplies the required energy and continues to discharge in this mode, as shown in Fig. 2 (e).

III. Design of Proposed PFC Converter

A 350 W PFC converter is designed for feeding a BLDC motor of 248 W (complete specifications of BLDC motor are mentioned in Appendix). The DC bus voltage of the PFC converter is controlled from 50V (V_{dcmin}) to 200V (V_{dcmax}).

The supply voltage (v_s) is given as,

$$v_S(t) = V_m Sin\left(2\pi f_L t\right) = 220\sqrt{2}\,Sin\left(314t\right)V \tag{1}$$

where V_m is amplitude of supply voltage i.e. 311V, and f_L is supply frequency i.e. 50Hz.

The average input rectified voltage is as [3],

$$V_{in} = \frac{2V_m}{\pi} = \frac{2\times 311}{\pi} \approx 198\,V \tag{2}$$

The output voltage, V_{dc} of the bridgeless Sheppard-Taylor converter (which belongs to buck-boost category) is as [3],

$$V_{dc} = \frac{D}{(1-D)}V_{in} \tag{3}$$

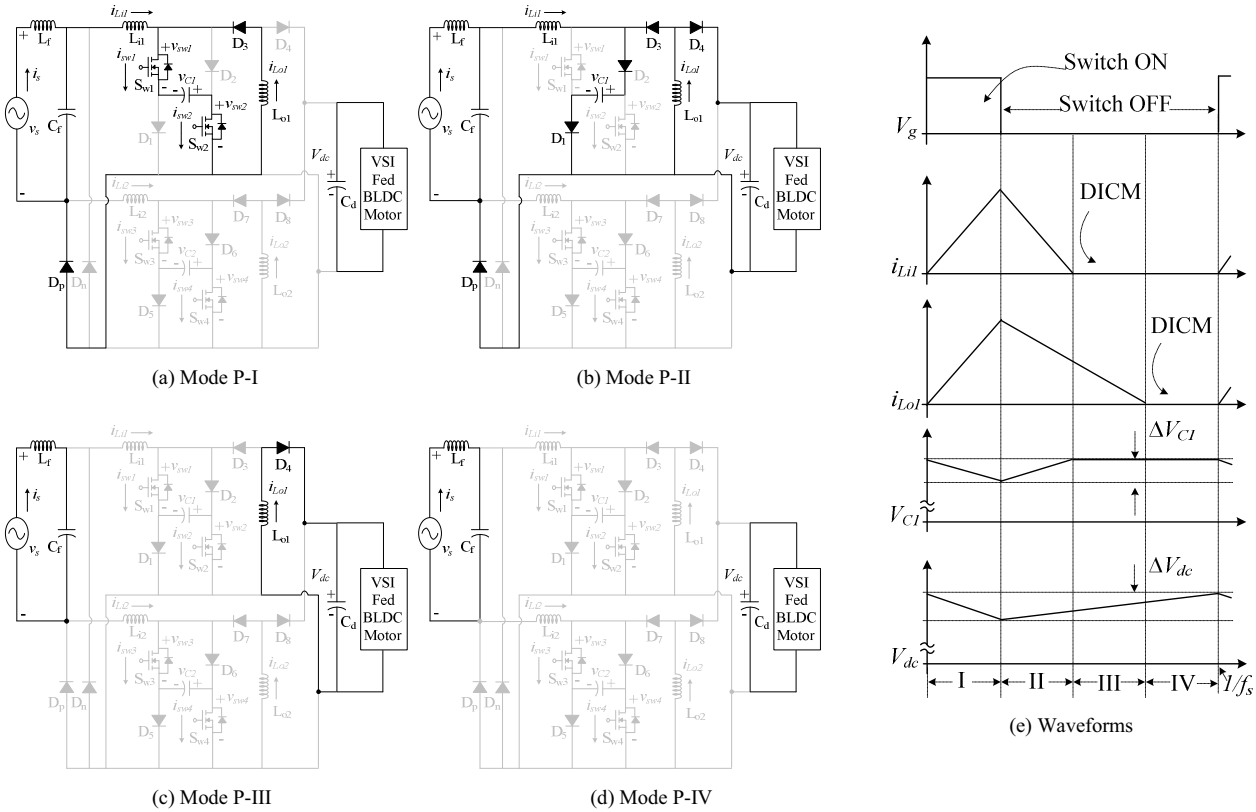
where D represents the duty ratio.

Hence the designed duty ratio D_{des}, corresponding to designed DC link voltage of V_{des} of 120 V is as,

$$D_{des} = \frac{V_{des}}{V_{in}+V_{des}} = \frac{120}{198+120} = 0.3774 \tag{4}$$

Now, a critical value of input inductor (L_i) is given as [6],

$$L_{ic} = \frac{D_{des}V_{in}}{f_S\left(2I_{in}\right)} = \frac{0.3374\times 198}{20000\times\left(2\times 350/198\right)} = 944.8\,\mu H \tag{5}$$



(a) Mode P-I (b) Mode P-II

(c) Mode P-III (d) Mode P-IV

(e) Waveforms

Fig. 2. (a-d) Different modes of operation of the proposed bridgeless Sheppard-Taylor converter and (e) the associated waveforms.

where I_{in} is input current and f_s is switching frequency which is selected as 20 kHz.

The input inductors (L_{i1} and L_{i2}) are chosen less than the critical value (L_{ic}) to operate in DCM. Hence it is selected around 1/3rd of critical value, i.e. $L_{i1} = L_{i2} = 300$ µH [15].

The critical value of output inductor (L_{oc}) is as [6],

$$L_{oc} = \frac{V_{des}\left(1 - D_{des}\right)}{f_S\left(2I_o\right)} = \frac{120\times(1-0.3774)}{20000\times\left(2\times 350/120\right)} = 681.53\,\mu H \quad (6)$$

The output inductors (L_{o1} and L_{o2}) are chosen less than the critical value (L_{oc}) to operate in DCM. Hence it is selected around 1/3rd of critical value, i.e. $L_{o1} = L_{o2} = 200$ µH [15].

Intermediate capacitor's (C_1 and C_2) are designed similar to SEPIC (Single Ended Primary Inductance Converter) as [6],

$$C_{1,2} = \frac{V_{des}D_{des}}{R_L f_S \Delta V_{C1}} = \frac{120\times 0.3774}{41.14\times 20000\times\left(0.3\times 318\right)} = 0.577\,\mu F \quad (7)$$

where R_L is the emulated load resistance i.e. V_{des}^2/P_o, and ΔV_{C1} is the allowable ripple in intermediate capacitor voltage, which is selected as 30% of intermediate capacitor voltage, V_C, where V_C is given as $V_C = V_{des}+V_{in}$. Hence, the intermediate capacitors are chosen as 0.6 µF.

The value of DC bus capacitor is calculated as [6],

$$C_d = \frac{I_d}{2\omega_L \Delta V_{des}} = \frac{\left(350/120\right)}{2\times 314\times 0.02\times 120} = 1935.2\,\mu F \quad (8)$$

where I_d is the DC link current and $\omega_L = 2\pi f_L$ where f_L is the line frequency and ΔV_{des} is acceptable ripple in DC link voltage which is chosen as 2 % of V_{des}.

Hence to ensure a smooth voltage at DC bus, the value of DC bus capacitor is selected as 2200 µF.

A LC filter is designed for suppressing the high harmonic current in the supply system due to high frequency switching [16]. The maximum value of filter capacitance C_{max} is as [16],

$$C_{max} = \frac{I_{peak}}{\omega_L V_{peak}} tan(\theta) = \frac{\left(350/220\sqrt{2}\right)}{314\times 311} tan(2^o) \approx 402.3nF \quad (9)$$

where I_{peak} and V_{peak} represent amplitude of supply current and supply voltage and θ represents the displacement angle.

The filter capacitance C_f is selected such that C_f is lower than C_{max}, Hence, a 330 nF capacitor is chosen for the filter.

The filter inductance L_f is expressed as [16],

$$L_f = \frac{1}{4\pi^2 f_c^2 C_f} = \frac{1}{4\pi^2\times 4000^2\times 330x10^{-9}} = 4.79\,mH \quad (10)$$

where f_c is cut-off frequency and is chosen as $f_c = f_s/5$ [16].

Hence the filter inductance (L_f) of 5 mH is selected for the required application.

IV. Control of The Proposed Drive

This section is divided into two sub-sections as control of a PFC converter for adjusting the DC bus voltage with PFC operation and control for BLDC motor to achieve an electronic commutation.

A. Control of PFC Converter

This section deals with the generation of high frequency PWM pulses for solid-state switches (S_{w1} and S_{w2}) of PFC converter. A voltage follower approach using a single voltage control loop is used for control of PFC converter. A reference voltage for DC bus capacitor (V_{dc}*) is as,

$$V_{dc}^{*} = k_v \omega^{*} \tag{11}$$

where k_v is motor voltage constant and ω* is reference speed.

This reference voltage (V_{dc}*) is compared with the sensed voltage of DC bus (V_{dc}) to generate the voltage error signal (V_e) as,

$$V_e(k) = V_{dc}^{*}(k) - V_{dc}(k) \tag{12}$$

where k represents the kth sampling instant.

This error voltage signal (V_e) is given to the voltage PI controller to generate a controlled output voltage (V_{cc}) as,

$$V_{cc}(k) = V_{cc}(k-1) + k_p\{V_e(k) - V_e(k-1)\} + k_i V_e(k) \tag{13}$$

where k_p and k_i represents the gains of the PI controller.

This voltage controller output (V_{cc}) and high frequency saw-tooth signal (m_d) are compared to generate PWM pulses as,

$$\left.\begin{array}{l} if\ m_d(t) < V_{cc}(t)\ then\ S_{w1} = S_{w2} = 'ON' \\ if\ m_d(t) \geq V_{cc}(t)\ then\ S_{w1} = S_{w2} = 'OFF' \end{array}\right\} for\ v_s > 0 \tag{14.a}$$

$$\left.\begin{array}{l} if\ m_d(t) < V_{cc}(t)\ then\ S_{w3} = S_{w4} = 'ON' \\ if\ m_d(t) \geq V_{cc}(t)\ then\ S_{w3} = S_{w4} = 'OFF' \end{array}\right\} for\ v_s < 0 \tag{14.b}$$

where S_{w1} - S_{w4} are PWM signals given to solid-state switches of the PFC converter.

B. Electronic Commutation of BLDC Motor

The BLDC motor is commutated electronically which includes proper switching of VSI, such that a symmetrical direct current is drawn from the DC bus for 120^0 and placed symmetrically at the centre of back-EMF of each phase. Hall-Effect position sensors are used for sensing the rotor position at a span of 60^0 for electronic commutation of BLDC motor. A line current i_{ab} is drawn from DC bus capacitor during the conduction of two switches (S_1 and S_4) as shown in Fig. 1. The magnitude of this current is decided by the DC bus voltage (V_{dc}), back-EMF's (e_{an} and e_{bn}), resistances (R_a and R_b) and self and mutual inductance (L_a, L_b and M) of the stator windings.

V. Results And Discussion

The performance evaluation of the proposed drive is carried for different speeds, supply voltages and loadings on the BLDC motor. Various parameters such as speed (ω), electromagnetic torque (T_e) and stator current (i_a) of BLDC motor are studied to demonstrate the performance of BLDC motor. Front end converter's parameters such as DC link voltage (V_{dc}), inductor's currents (i_{Li1}, i_{Li2}, i_{Lo1} and i_{Lo2}) and intermediate capacitor's voltage (V_{C1} and V_{C2}) are also evaluated for study the proper functioning of the PFC converter. Power quality assessment of the proposed drive is carried out on the basis of various PQ indices such as power factor (*PF*), displacement power factor (*DPF*), crest factor (*CF*) and total harmonic distortion (*THD*) of supply current at AC mains. Switches stress in terms of peak voltage (V_{sw}) and peak current (I_{sw}) of switch are also studied for deciding the rating of PFC converter's switches.

A. Performance During Steady State Operation

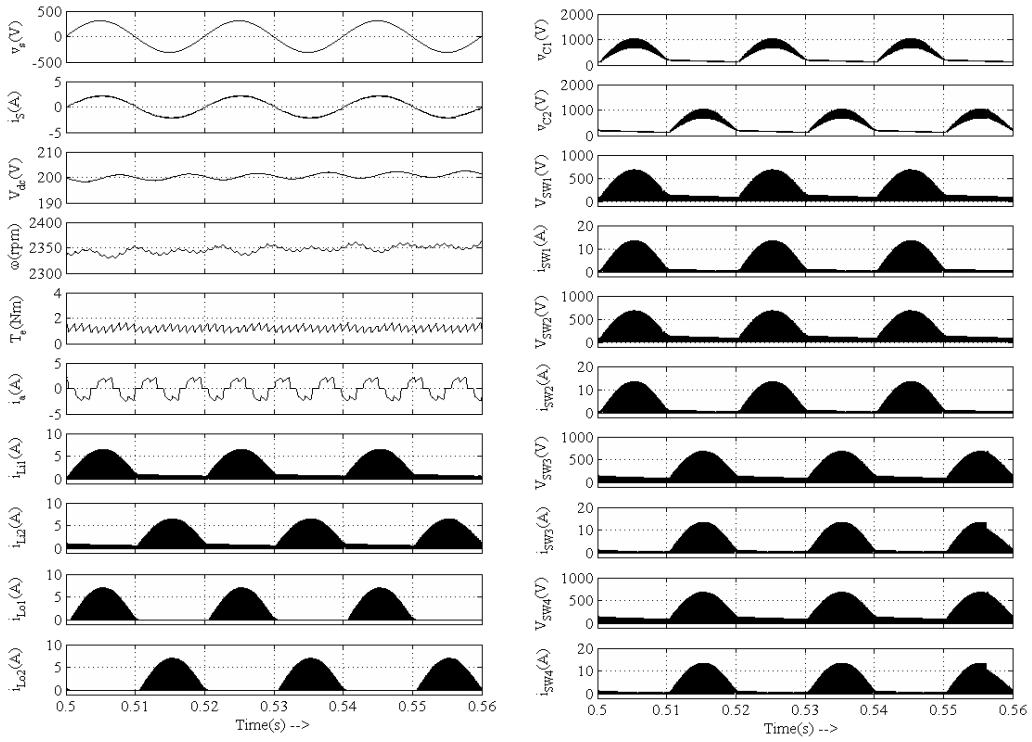
Figs. 3 (a) and 3 (b) show the steady state operation of the proposed drive. As shown in these figures, a sinusoidal current is obtained in phase with supply voltage which clearly indicates a unity power factor operation. Moreover, discontinuous currents in input and output inductor (i_{Li1}, i_{Li2}, i_{Lo1} and i_{Lo2}) and continuous intermediate capacitor's voltage (V_{C1} and V_{C2}) are achieved which shows the operation of PFC converter in DCM. An acceptable voltage and current stress of the order of 650 V, 15 A is achieved on the PFC converter switches. Figs. 4 (a) and (b) show the supply current's harmonic spectra for the BLDC motor operating at rated condition with supply voltage as 220V and DC bus voltage as 200 V and 50 V respectively. Acceptable power quality indices have been obtained within IEC 61000-3-2 limits [4].

B. Performance During Supply Voltage Fluctuation

Figs. 4 (c) and (d) show the supply current's harmonic spectra at AC mains for the BLDC motor operating at rated condition with DC link voltage as 200 V and supply voltage as 170 V and 270 V respectively. A unity power factor of the proposed drive is also obtained at wide range of supply voltage fluctuations.

C. Dynamic Behaviour of the Proposed Drive

Fig. 5 (a) shows the starting of BLDC motor at step change in DC link voltage from 0 V to 50 V. Fig. 5 (b) shows the dynamic behavior of during speed control of proposed bridgeless Sheppard-Taylor converter fed BLDC motor drive corresponding to change in DC link voltage from 100 V to 150 V. The performance of the proposed drive is also evaluated corresponding to step change in load from 0.4 Nm to 0.8 Nm on BLDC motor is shown in Fig. 5 (c). Moreover, the dynamic behaviour of the proposed bridgeless Sheppard-Taylor converter fed BLDC motor drive during supply voltage fluctuation from 270 V to 170 V is shown in Fig. 5 (d). The DC bus voltage is maintained at the desired value thus demonstrating a satisfactory closed loop performance.



(a) (b)

Fig. 3. Performance of the proposed drive at steady state operation.

VI. CONCLUSION

A PFC based bridgeless Sheppard-Taylor converter has been proposed for feeding BLDC motor drive. The speed of proposed drive has been controlled via a single voltage sensor with power factor correction at AC mains. An approach of variable voltage at DC bus of the VSI has been used for speed control of BLDC motor. Moreover, the VSI has been operated in low frequency switching for reducing the switching losses in the VSI. The proposed bridgeless Sheppard-Taylor converter has been designed to operate in DCM for inherent power factor correction. The proposed drive has shown a unity power factor at AC mains over a wide range of speed control. The obtained power quality indices have been observed within IEC 61000-3-2.

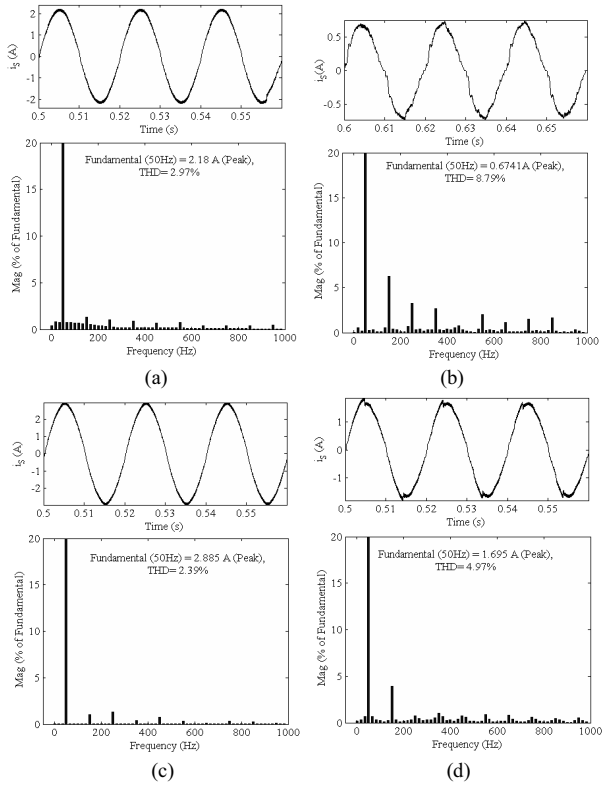
APPENDIX

BLDC Motor Rating: 4 pole, P_{rated} (Rated Power) = 248.7 W, V_{rated} (Rated DC link Voltage) = 200 V, T_{rated} (Rated Torque) = 0.9473 Nm, ω_{rated} (Rated Speed) = 2500 rpm, K_v (Voltage Constant) = 62 V/krpm, K_t (Torque Constant) = 0.6641 Nm/A, R_{ph} (Phase Resistance) = 3.4 Ω, L_{ph} (Phase Inductance) = 25.71 mH, J (Moment of Inertia) = 1.8×10^{-4} Nm/s.

Controller Gains: $K_p = 0.3$, $K_i = 0.001$.

REFERENCES

[1] C. L. Xia, *Permanent Magnet Brushless DC Motor Drives and Controls*, Wiley Press, Beijing, 2012.



(a) (b) (c) (d)

Fig. 4. Harmonic spectra of supply current at AC mains for BLDC motor operated at rated loading and (a) $V_s = 220$ V, $V_{dc} = 200$ V, (b) $V_s = 220$ V, $V_{dc} = 50$ V, (c) $V_s = 170$ V, $V_{dc} = 200$ V and (a) $V_s = 270$ V, $V_{dc} = 200$ V.

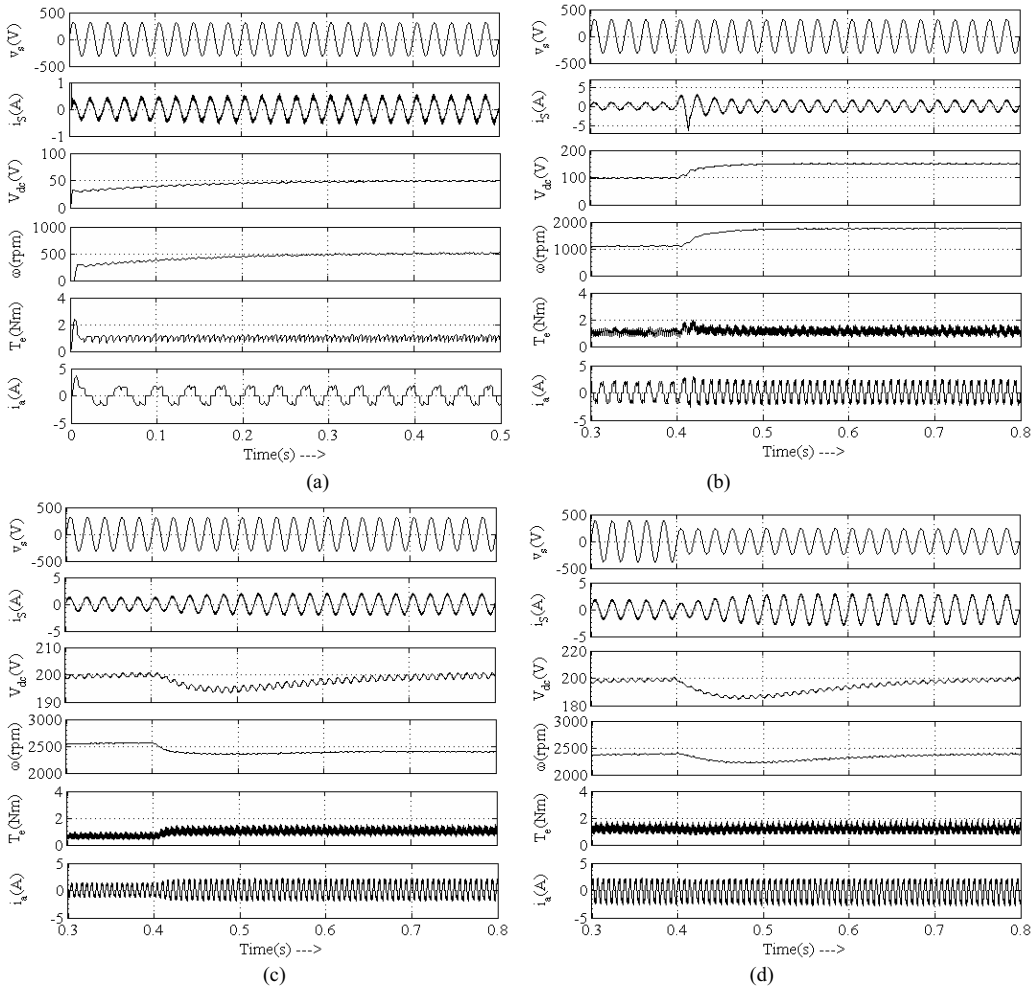


Fig. 5. Operation of the proposed drive during (a) stating at V_{dc} = 50 V, (b) speed control at change in DC bus voltage from 100 V to 150 V (c) change in load from 0.4 Nm to 0.8 Nm and (d) supply voltage variation from 270 V to 170 V.

[2] H. A. Toliyat and S. Campbell, *DSP-based Electromechanical Motion Control*, CRC Press, New York, 2004.

[3] N. Mohan, T. M. Undeland and W. P. Robbins, *Power Electronics: Converters, Applications and Design*, Wiley Pub., USA, 2009.

[4] *Limits for Harmonic Current Emissions (Equipment input current ≤ 16A per phase),* International Standard IEC 61000-3-2, 2000.

[5] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey and D.P. Kothari, "A review of single-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Elect*.,vol.50,no.5,pp.962– 981,Oct. 2003.

[6] B. Singh, S. Singh, A. Chandra and K. Al-Haddad, "Comprehensive Study of Single-Phase AC-DC Power Factor Corrected Converters With High-Frequency Isolation," *IEEE Trans. Ind. Inform.*, vol.7, no.4, pp.540-556, Nov. 2011.

[7] T. Y. Ho, M. S. Chen, L. H. Yang and W. L. Lin, "The Design of a High Power Factor Brushless DC Motor Drive," *2012 Int. Sympo. Computer, Consumer and Control,* pp.345-348, 4-6 June 2012.

[8] T. Gopalarathnam and H. A. Toliyat, "A new topology for unipolar brushless DC motor drive with high power factor," *IEEE Trans. Power Electron.*, vol.18, no.6, pp. 1397- 1404, Nov. 2003.

[9] B. Singh and V. Bist, "Power Quality Improvements in PFC Luo Converter Fed BLDC Motor Drive", *Int. Trans. Elect. Energy Sys.,* vol. 24, no. 5, pp.1-22, Feb. 2014.

[10] B. Singh and V. Bist, "An Improved Power Quality Bridgeless Cuk Converter Fed BLDC Motor Drive for Air Conditioning System", *IET Power Electronics*, Vol. 6, no. 5, pp. 902–913, May 2013.

[11] V. Bist and B. Singh, "A Reduced Sensor PFC BL-Zeta Converter Based VSI Fed BLDC Motor Drive", *Electric Power System Research,* vol. 98, pp. 11–18, May 2013.

[12] H. Y. Kanaan and K. Al-Haddad, "A modified Sheppard-Taylor power factor corrector operating in Discontinuous Capacitor Voltage Mode," *Proc. of IEEE Int. Sympos. on Ind. Electron. (ISIE),* pp.81-88, 27-30 June 2011.

[13] A. Karaarslan, "The Implementation of Bee Colony Optimization Algorithm to Sheppard–Taylor PFC Converter," *IEEE Trans. Ind. Electron.*, vol.60, no.9, pp.3711-3719, Sept. 2013.

[14] E. H. Ismail, A. J. Sabzali and M. A Al-Saffar, "A High-Quality Rectifier Based on Sheppard–Taylor Converter Operating in Discontinuous Capacitor Voltage Mode," *IEEE Trans. Ind. Electron.*, vol.55, no.1, pp.38-48, Jan. 2008.

[15] D. S. L. Simonetti, J. Sebastian and J. Uceda, "The discontinuous conduction mode Sepic and Cuk power actor preregulators: analysis and design," *IEEE Trans. Ind. Elect.*, vol. 44, no. 5, pp. 630-637, Oct. 1997.

[16] V. Vlatkovic, D. Borojevic and F. C. Lee, "Input Filter Design for Power Factor Correction Circuits," *IEEE Trans. Power Electron.*, vol.11, no.1, pp.199-205, Jan 1996.