# Pulse Width Modulation Scheme fora Quasi Six-Phase Voltage Source Inverter

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**Abstract: In this paper, a simple voltage modulation technique is described for a quasi six-phase voltage source inverter (VSI). The proposed modulation is based on the sampled reference voltages and effective time concept. In the proposed technique the actual switching times for each inverter legs are obtained directly in simple form. The execution time in real time application can be reduced significantly compared to the conventional space vector pulse width modulation (SVPWM). Simulation and experimental results are provided to validate the proposed theory.**

*Keywords – Six-phase inverter, Dual three-phase, Time equivalent SVPWM.*

## I INTRODUCTION

The multi-phase variable speed electric drive was proposed in late 1960s. Since then the pace of development was steady but relatively slow and limited during the first three decades of its inception. The situation has, however, changed in the last decade, when an upsurge in the research effort in this area took place. The driving forces behind this accelerated development have been specific application areas: railway traction and electric vehicle/hybrid electric vehicle applications, "more-electric" aircraft and electric ship propulsion [1]. The reasons for employing multi-phase drives vary from application to application and range from reduction of the converter per phase rating to significantly improved fault tolerance. Since in variable-speed ac drives an electric machine is supplied using a power electronic converter, the number of phases is no longer restricted to three. Hence, the machine and the power electronic converter can be built with any number of phases appropriate to the specific application. The recent developments in the area of multi-phase machines and drives have been supported by advances in power semiconductor devices and DSPs. Detailed reviews on the development in the area of multi-phase drive research is published in recent past [2-6].

Many industrial applications require precise control algorithms of power electronic converters. Growing interest is found towards the Pulse width modulation techniques for power inverters. A variety of modulation techniques for quasi six-phase inverters have been developed in the recent past [7-22]. Among many modulation strategies, spacevector pulse width modulation techniques have seen more attention from the researcher. For the AC machine drive application, full dc bus voltage utilization is important in order to achieve maximum torque under all operating conditions. This is achieved in the space vector PWM. Nevertheless, the output of space vector PWM inverter contains lower order harmonics. It is indicated in the literature that it is not possible to completely eliminate these harmonics in a quasi six-phase inverter [6].

This paper thus proposes a voltage modulation method to provide sinusoidal output with improved dc bus utilization. The major contribution of this paper is to offer higher dc bus utilisation compared to the carrier based PWM and equal to the value obtainable with the space vector PWM and provide completely sinusoidal output similar to the carrier based PWM. In this paper, a novel voltage modulation scheme is described. From the concept of "effective voltage" similar to [8], the actual switching time for each inverter legs are deduced directly in a simple form. The proposed PWM method has the high performance voltage generation capability exactly same as the conventional space vector PWM method.

## II MODELLING OF SIX-PHASE INVERTER - A REVIEW

The power circuit of a quasi six-phase VSI is shown in Fig. 1. Each switch consists of a power switching device such as IGBT or MOSFET in parallel to a snubber circuit. Since six dependent currents can flow in a general case, therefore, this is a six dimensional system. Thus modeling and control problems of such system must be addressed from the point of six dimensional spaces. The inverter input dc voltage is treated as constant. The load is star-connected (dual three-phase) with isolated neutrals as shown in Fig. 1. The inverter output phase voltages are denoted in Fig. 1 with lower case symbols (*a,,b,c,d,e,f*), while the pole voltages have symbols in capital letters (*A,B,C,D,E,F*).

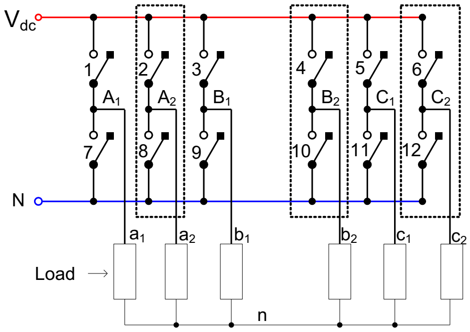


Fig. 1 Power circuit of asymmetrical six-phase voltage source inverter

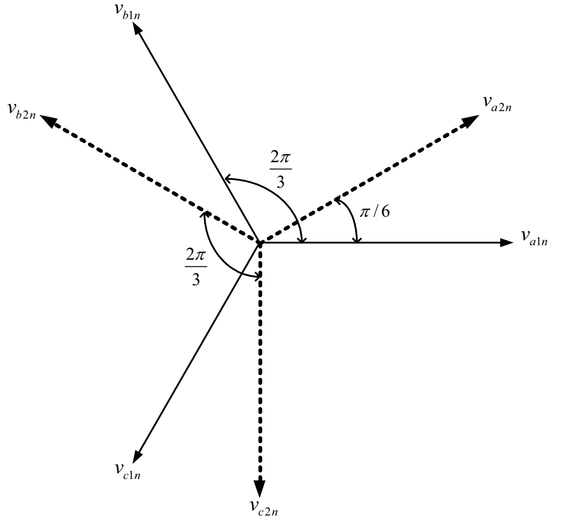


Fig. 2. Phasors of phase-to-neutral voltages for quasi six-phase system

The relationship between the inverter phase-to-neutral voltages and inverter pole voltages is obtained as;

$$\begin{aligned}
v_a &= (5/6)v_A - (1/6)(v_B + v_C + v_D + v_E + v_F) \\
v_b &= (5/6)v_B - (1/6)(v_A + v_C + v_D + v_E + v_F) \\
v_c &= (5/6)v_C - (1/6)(v_A + v_B + v_D + v_E + v_F) \\
v_d &= (5/6)v_D - (1/6)(v_A + v_B + v_C + v_E + v_F) \qquad (1) \\
v_e &= (5/6)v_E - (1/6)(v_A + v_B + v_C + v_D + v_F) \\
v_f &= (5/6)v_F - (1/6)(v_A + v_B + v_C + v_D + v_E)
\end{aligned}$$

where the inverter pole voltages take the values of $\pm\, 0.5V_{DC}$.. In general, an $n$ phase two level VSI has a total $2^n$number of switching states. Therefore for a six-phase VSI, total number of switching states is 64, in which four are zero vectors and the remaining 60 are active vectors. By using decoupling transformation matrix given in (2) each voltage vector can be decomposed into three orthogonal two dimensional subspaces *d-q*,*x-y* and $o_1$-$o_2$. The $o_1$-$o_2$are equal to zero because the neutrals $n_1$ and $n_2$ are assumed isolated. Thus this pair of vectors is omitted from further discussion. The modulation techniques thus confines to the two remaining orthogonal sub-spaces *d-q* and *x-y*.

$$[T] = \frac{2}{6}\begin{bmatrix} 1 & \cos(\theta) & \cos(4\theta) & \cos(5\theta) & \cos(8\theta) & \cos(9\theta) \\ 0 & \sin(\theta) & \sin(4\theta) & \sin(5\theta) & \sin(8\theta) & \sin(9\theta) \\ 1 & \cos(5\theta) & \cos(8\theta) & \cos(\theta) & \cos(4\theta) & \cos(9\theta) \\ 0 & \sin(5\theta) & \sin(8\theta) & \sin(\theta) & \sin(4\theta) & \sin(9\theta) \\ 1 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 \end{bmatrix} \qquad (2)$$

$$\underline{v}_{dq} = \frac{2}{6}(v_a + \underline{a}v_b + \underline{a}^4 v_c + \underline{a}^5 v_d + \underline{a}^8 v_e + +\underline{a}^9 v_f) \qquad (3)$$

$$\underline{v}_{xy} = \frac{2}{6}(v_a + \underline{a}^5 v_b + \underline{a}^8 v_c + \underline{a}v_d + \underline{a}^4 v_e + \underline{a}^9 v_f) \qquad (4)$$

where$\underline{a}$= $exp(\pi/6)$. Fig. 2 represents the space vector representation of all the vectors in *d-q* axis and Fig. 3 represents in *x-y* axis. All the zero vectors are at the origin so that a vector can be represented in six dimensional spaceas shown in figures 3& 4, according to the largest vectors lie at the vertices of the polygon there are total twelve $\pi/6$ radian sectors.

## CONVENTIONAL SPACE VECTOR PWM SCHEMES

It is shown in [10] that for an $n$ phase inverter, the minimum ($n$-1) numbers of vectors are required to synthesize the input reference and the output obtained is sinusoidal in nature. Therefore, following the same principle for a six-phase inverter minimum number of vectors required for sinusoidal output is five.

There are numerous methods of choosing vectors so that they have maximum amplitude on *d-q* axis and minimum amplitude on *x-y* axis [10-11]. In the most simple form of space voltage PWM, only those switching states vectors , which lie at the vertices of the polygon as shown in Fig. 3 are employed to synthesize the reference vector ($V^*$). Two active vectors of largest length and zero vectors are used during one sampling interval [3]. This is similar to the one used in a three-phase VSI. However, this scheme when employed in a six-phase VSI leads to unwanted low-order harmonics due to the presence of the space vectors in *x-y* plane.

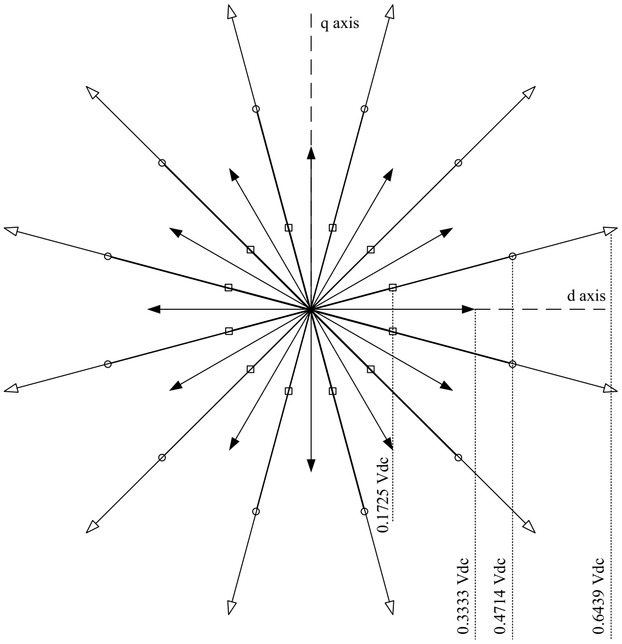


Fig. 3 Space vector representation of all the vectors in *d-q* axis

Another method is the vector space decomposition scheme proposed by Y. Zhao [9], in this method four adjacent voltage vectors are always selected which spans the outer most polygon on the *d-q* plane according to the position of the reference voltage vector $V^*$, the fifth vector is chosen from the zero vector located at the origin of the *d-q* plane as shown in

Fig. 3. Space vector PWM strategy is accomplished by the following equation

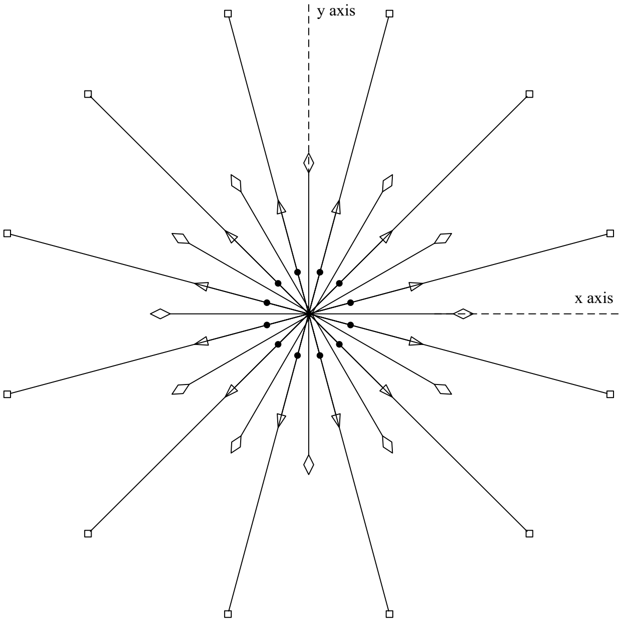


Fig. 4 Space vector representation of all the vectors in $x$-$y$ axis

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \end{bmatrix} = \begin{bmatrix} V_d^{\,1} & V_d^{\,2} & V_d^{\,3} & V_d^{\,4} & V_d^{\,5} \\ V_q^{\,1} & V_q^{\,2} & V_q^{\,3} & V_q^{\,4} & V_q^{\,5} \\ V_x^{\,1} & V_x^{\,2} & V_x^{\,3} & V_x^{\,4} & V_x^{\,5} \\ V_y^{\,1} & V_y^{\,2} & V_y^{\,3} & V_y^{\,4} & V_y^{\,5} \\ 1 & 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} V_d^{\,*}T_s \\ V_q^{\,*}T_s \\ 0 \\ 0 \\ T_s \end{bmatrix} \qquad (5)$$

Where $V_x^k$is the projection of the $k^{th}$ voltage vector on the $x$ axis and $T_k$ is the dwell time of that vector during time interval $T_s$. The quantities $V_d^*$ and $V_q^*$ are the $d$-$q$ plane reference voltages. During each sampling period $T_s$, a set of five voltage vectors must be chosen to guarantee that each $T_k$ has positive and unique solution. Although the current harmonics are suppressed but the computation time required to implementing this method is considerably large.

Three largest vectors and one smaller vector, used in vector classification algorithm [11], which is a generalized conventional SVPWM. The vectors used in SPWM and the SVPWM method based on unified modulation method proposed by L. Ching [13], where three largest vectors and two smaller vectors are chosen automatically. The implementation of this scheme is easier but the drawback of this method is higher switching losses.

Another method proposed by K. Marouani [14], PWM strategy based on 24 sectors. This technique combines the maximum magnitude $d$-$q$ plane voltage vectors and the ones with half magnitudes. These voltage vectors divide the $d$-$q$ plane into twenty four $\pi/12$ radian sectors. In each sampling period, the reference voltage vector is achieved by selecting a set of three voltage vectors among those have maximum magnitude and fourth vector among the ones with half magnitude. This method once again suffers from the drawback of larger computational time.

## III TIME EQUIVALENT SPACE VECTOR PWM SCHEME

The presented modulation scheme called here “Time equivalent space vector PWM (TESVPWM)” utilises simply the sampled reference voltages to generate the gating time for which each inverter leg to yield sinusoidal output. This method is an extension of the technique developed in [2] for a three-phase VSI. The major advantage offered by the proposed scheme is its flexible nature as relocation of “effective time” within the switching period results in various types of PWM scheme such as carrier-based, SVPWM and discontinuous modulation. Additionally the computation time is greatly reduced as the sector identification and reference of lookup table is not used in the proposed algorithm contrary to the SVPWM techniques elaborated in the previous section. In the proposed algorithm the reference voltages are sampled at fixed time interval equal to the switching time. The sampled amplitudes are converted to equivalent time signals. The time signals thus obtained are imaginary quantities as they will be negative for negative reference voltage amplitudes. Thus a time offset is added to these signals to obtain the gating time of each inverter leg. This offset addition centres the active switching vectors within the switching interval offering high performance PWM similar to SVPWM. The algorithm is given below,Where $Vx$; $x=a,b,c,d,e,f$; is the sampled amplitudes of reference phase voltages during sampling interval and $T_s$ is the inverter switching period. $Tx;x=a,b,c,d,e,f$; are referred as time equivalents of the sampled amplitudes of reference phase voltages. $T_{max}$ and $T_{min}$ are the maximum and minimum values of $Tx$ during sampling interval. $T_o$is the time duration for which the zero vectors is applied in the switching interval. $T_{offset}$ is the offset time when added to time equivalent becomes gating time signal or the inverter leg switching time $T_{gx,}x=a,b,c,d,e,f$ [8].

*Algorithm of the proposed TESVPWM:*

I Sample the reference voltages $V_a$ ,$V_b$, $V_c$, $V_d$, $V_e$& $V_f$ in every switching period $T_s$.

II Determine the equivalent times $T_1$,$T_2$, $T_3$,$T_4$, $T_5$& $T_6$ given by expreesion, where $x$ $a,b,c,d,e$ and $f$;

$$T_{xs} = V_{xs} \times \frac{T_s}{V_{dc}};$$

III Determine $T_{offset;}$ $T_{offset} = \frac{T_S}{2} - \frac{T_{\max} + T_{\min}}{V_{dc}}$

IV Then the inverter leg switching times are obtained as $T_{gx} = T_x + T_{offset;}$ x =$a,b,c,d,e$ and $f$.

Fig. 5 shows the principal of Time Equivalent method for asymmetrical six-phase, if one fundamental cycle of modulating signal is divided into ten equal parts (sectors) and sampling is done in the first part then the equivalent mathematical analysis for first part is given below and on the basis of this analysis the equivalent switching wave form is shown in Fig. 6.

**Sector 1**

$$T_{\max} = T_a \,; T_{\min} = T_d \,;$$

$$T_1 = T_a - T_f \,; T_2 = T_f - T_b \,; T_3 = T_b - T_e \,; T_4 = T_e - T_c \,;$$

$$T_5 = T_c - T_d \,; T_{effective} = T_{\max} - T_{\min} \,; = T_a - T_d \,;$$

$$T_0 = T_s - T_{effective} \,; T_{offset} = \frac{T_0}{2} - T_{\min} = \frac{T_0}{2} - T_d \,;$$

$$T_{ga} = T_a + T_{offset} = T_a + \frac{T_0}{2} - T_d = \frac{T_0}{2} + T_1 + T_2 + T_3 + T_4 + T_5$$

$$T_{gb} = T_b + T_{offset} = T_b + \frac{T_0}{2} - T_d = \frac{T_0}{2} + T_3 + T_4 + T_5 \,;$$

$$T_{gc} = T_c + T_{offset} = T_c + \frac{T_0}{2} - T_d = \frac{T_0}{2} + T_5 \,;$$

$$T_{gd} = T_d + T_{offset} = T_d + \frac{T_0}{2} - T_d = \frac{T_0}{2} \,;$$

$$T_{ge} = T_e + T_{offset} = T_e + \frac{T_0}{2} - T_d = \frac{T_0}{2} + T_4 + T_5 \,;$$

$$T_{gf} = T_f + T_{offset} = T_f + \frac{T_0}{2} - T_d = \frac{T_0}{2} + T_2 + T_3 + T_4 + T_5 \,;$$

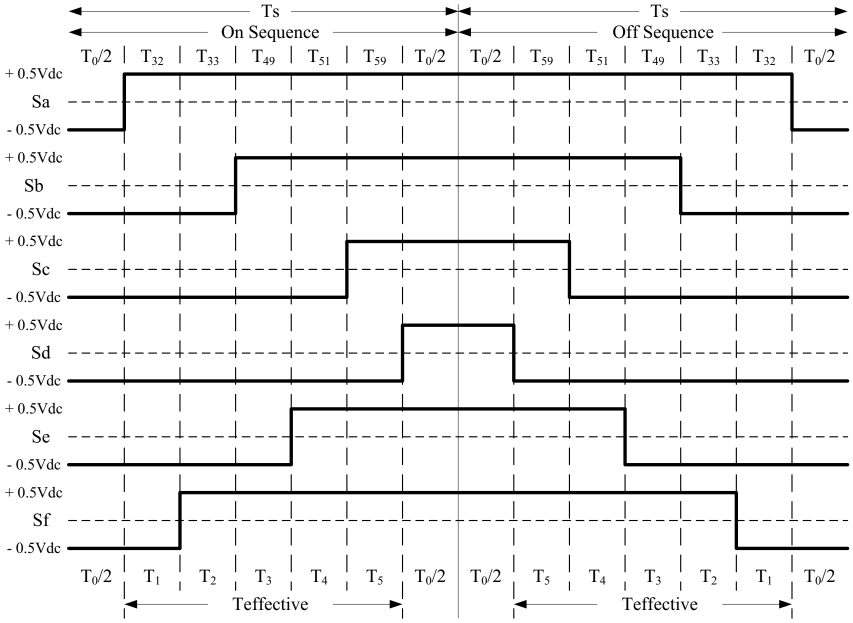


Fig. 6 switching waveforms for sector 1 using the proposed TESVPWM

From the switching waveform of Fig. 6, for first part the space vectors used are 32,33,49,51 and 59 for the implementation of modulation scheme. Their positions in the *d-q* plane can be seen in Fig. 3 and in *x-y* plane in Fig. 4. The vectors used in all the sectors and their order of switching are given in Table 1.

The proposed TESVPWM is simulated using Matlab/Simulink model shown in Fig. 7. The asymmetric six-phase voltage is provided with amplitude equals to ± 0.5 $V_{DC}$ and $V_{DC}$ is kept unity. The switching frequency is chosen equal to 5 KHz.

Table 1 Vectors used for SVPWM in different sectors

| Sector No. | Vectors |
|---|---|
| 1 | 32,33,49,51,59 |
| 2 | 32,48,49,51,59 |
| 3 | 16,48,56,60,61 |
| 4 | 16,24,56,60,61 |
| 5 | 8,12,28,60,62 |
| 6 | 4,12,14,30,31 |
| 7 | 4,12,14,15,31 |
| 8 | 2,3,7,15,47 |
| 9 | 2,3,7,39,47 |
| 10 | 1,3,35,51,55 |

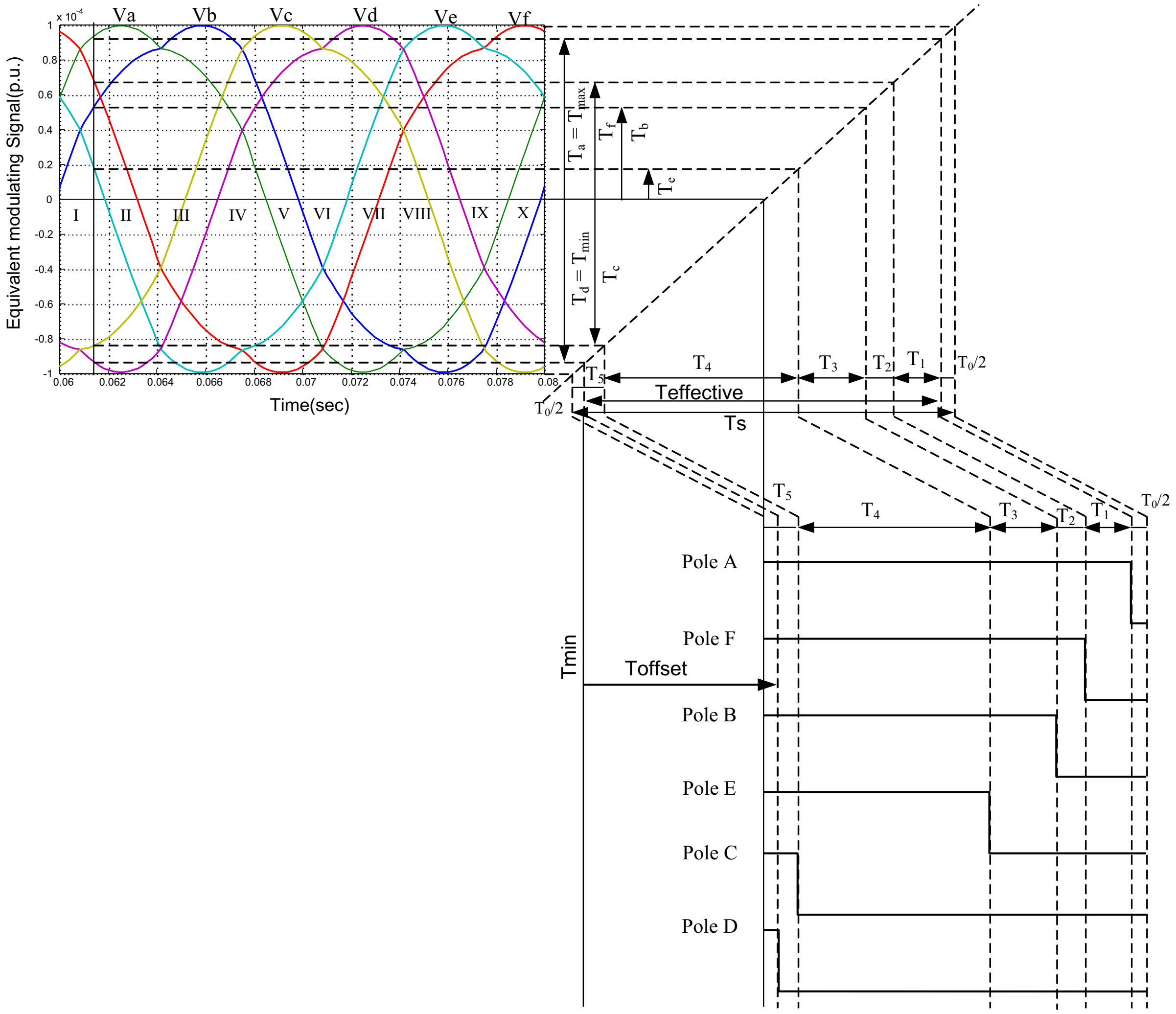


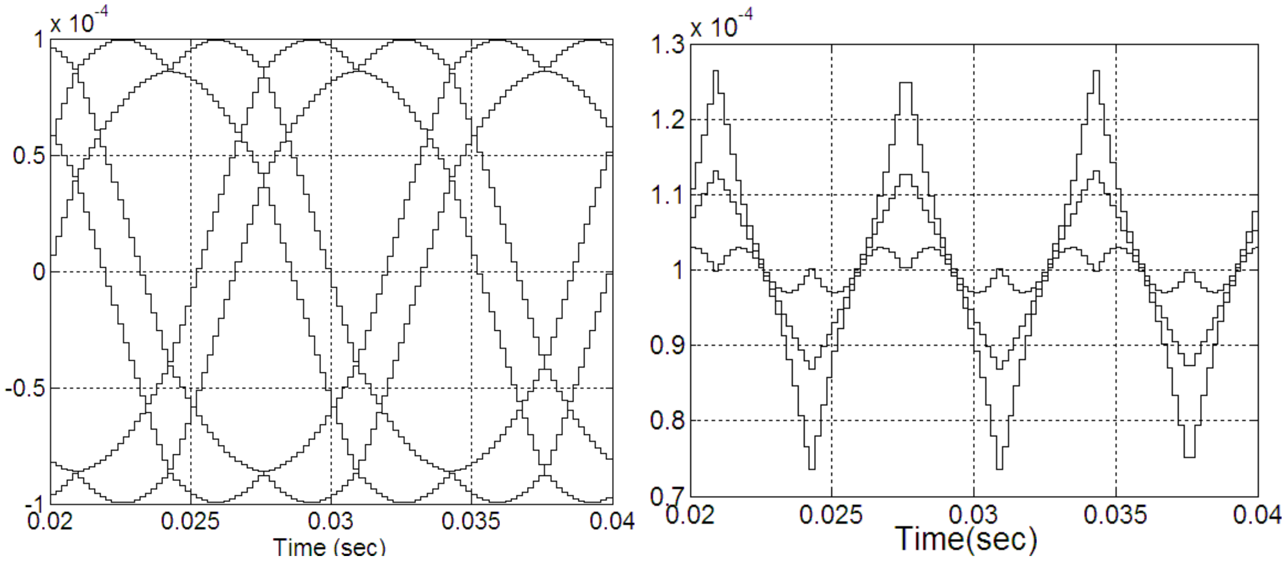
Fig. 5 Principal of TESVPWM for sector 1

## V SIMULATION RESULTS

Simulation results are provided in Fig. 7. The modulation signal voltages are shown in Fig.7 (a) and the equivalent offset time signals are calculated according to algorithm are shown in Fig. 7 (b). The output phase ‘a’ current in a R-L load is depicted in Fig. 7 (c) and Fig. 7 (d) shows the harmonic spectrum for phase ‘a’. The maximum modulation index obtained here is 0.515.

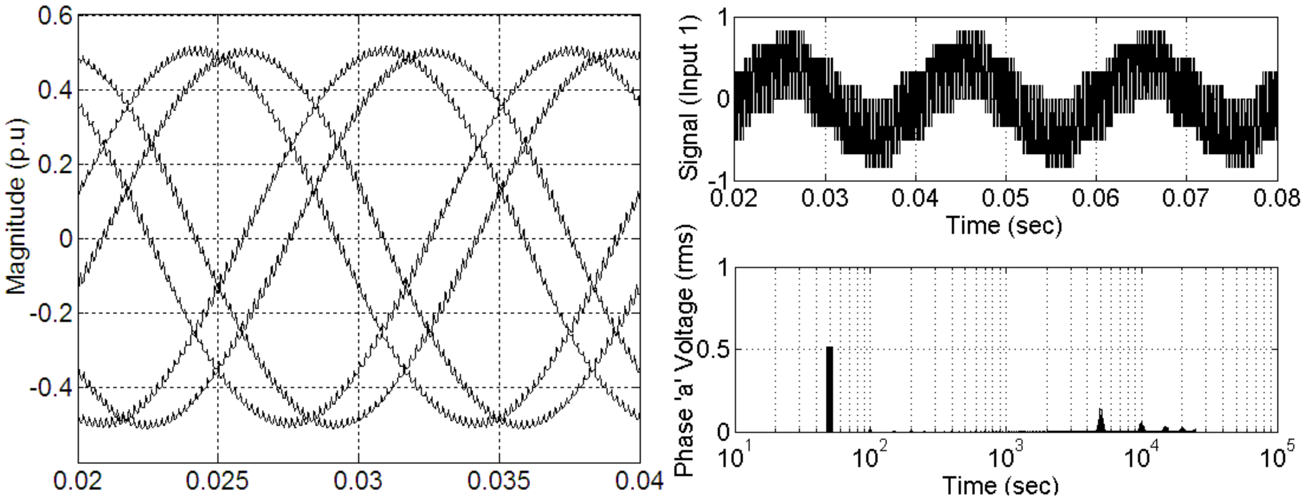
## VI EXPERIMENTAL INVESTIGATION

Experimental investigation is performed to implement the proposed scheme for a quasi-six phase VSI.The DC link is paralleled to make it common for all the modules. The DSP TMS320F2812 has provision of generating four independent PWM outputs per event manager thus a maximum of eight-phase inverter can be controlled using one DSP. Outof five PWM, three are generated using full compare units and the other one is generated by the GP timer compares units. The full compare unit has programmable dead-band for PWM output pairs but the other one PWM channel does not have the provision of dead band. Thus a dead band generating circuit is fabricated which act upon those PWM signals which do not have inbuilt dead band. A distribution panel is developed which distributes the fourteen PWM signals generated from DSP to three power modules. Fig. 9 and Fig. 10 shows the experimental resultsof a DSP based quasi-six phase VSI. Fig 10(a) shows the filtered PWM signals and 10 (b) shows the switching waveforms of the PWM signals. Fig 11(a) shows the output of the PWM inverter and 11(b) shows the harmonic spectrum of the phase ‘a’ voltage.



(a) Modulating signals

(b) Equivalent offset times signals



(d) Filtered output current

(e) Harmonic spectrum phase ‘a’ voltage

Fig. 7 Simulation results of TESVPWM scheme for asymmetric six-phase VSI

Fig. 8 The quasi-six phase voltage source inverter set-up

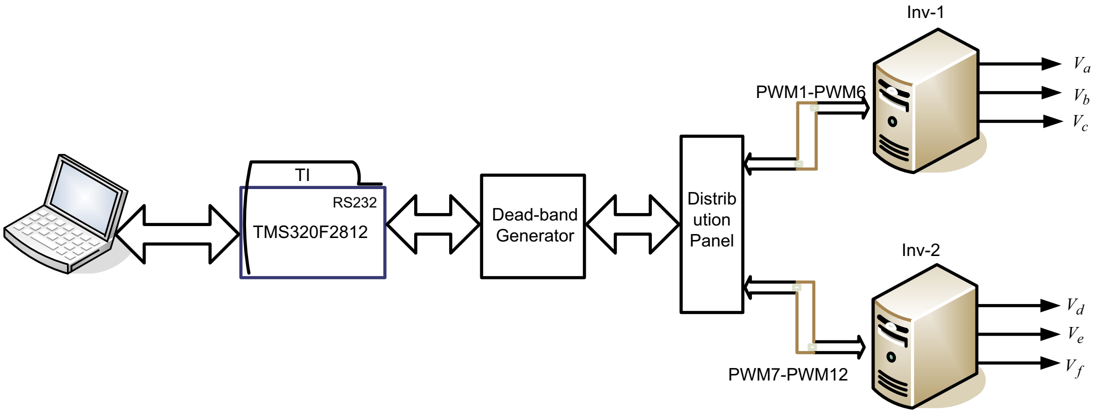


Fig. 9 Block schematic of a DSP based quasi-six phase VSI.

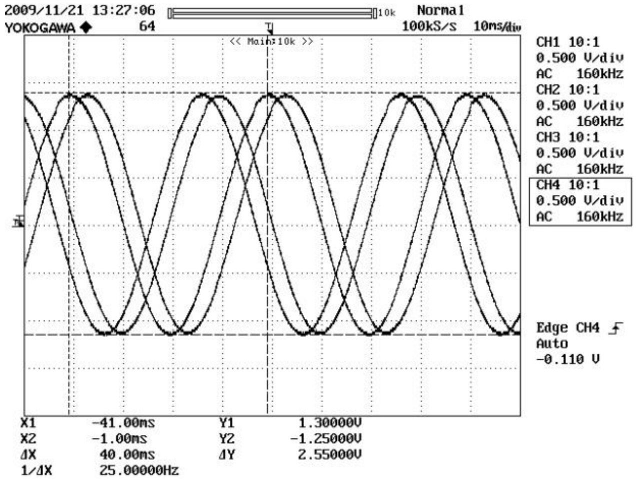


Fig. 10(a)Filtered PWM signal

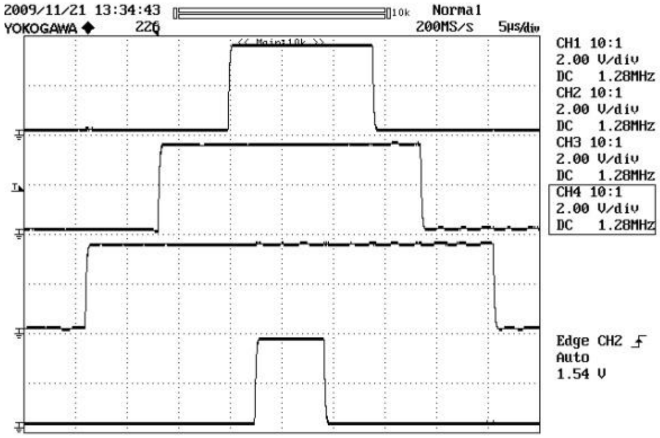


Fig. 10(b) switching waveforms for the PWM signals

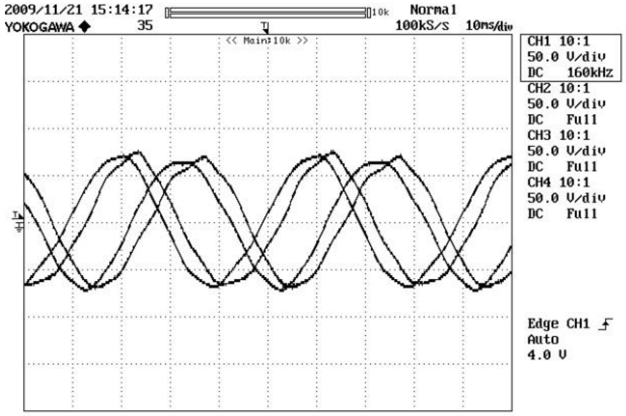


Fig. 11(a) Output of the PWM inverter

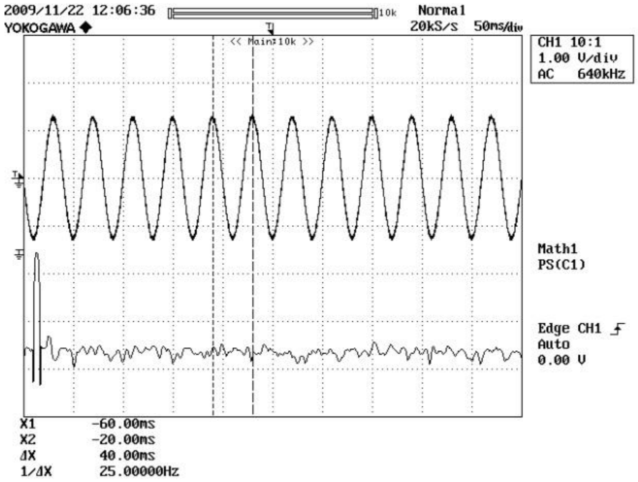


Fig. 11(b) harmonic spectrum of phase ‘a’voltage

## VII CONCLUSION

In this paper a simple voltage modulation technique is presented and is designated as time equivalent SVPWM. In the proposed method, reference space vector is sampled at a regular interval to determine the inverter switching vectors and their time durations in a sampling interval. These equivalent times are then converted to the actual gating time of each leg. In comparison with the present convention SVPWM schemes, in the proposed scheme, there is no need to look for sectors, vectors, lookup tables and no need to calculate the time of application for switching vectors. The proposed method offers a simple approach to realise the complex SVPWM algorithm. The output obtainable has the same quality as that of the conventional SVPWM. The proposed TESVPWM offers major advantages in real time DSP implementation due its computational efficiency. The Matlab/Simulink implementation and their simulation results are provided. Experimental results have given for the validity of the concept.

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