Structural and Electrical properties of modified CMOS Device under Radiation Environment in Designing of Voltage Control Oscillator (VCO)

C P Jain
Department of Electronics, Banasthali University,
Banasthali, Rajasthan,
India-304022
cpjain.vlsi@gmail.com

***Abstract*—This paper shows the structural CMOS with and without radiation and variation of electrical properties of device under various radiations doses and proposes a modified CMOS circuit which mitigates radiation effect by improving switch point in I-V characteristic. In order to redesign the circuit for radiation resistance; the above radiation hardened inverter circuit is used to design the Voltage Controlled Oscillator using Radiation Hardened By Design (RDBD) technique. The circuit exhibits only minimal degradation with total dose when irradiated.**

Keywords*— Radiation Hardened By Design (RHBD), single event transients, total ionizing dose, Voltage Controlled Oscillators (VCO).*

1. INTRODUCTION

There is an abundance of photonic and particulate radiation in outer space. Depending on the energy of the particles, they affect semiconductor devices differently. X-Ray, Gamma Ray and heavy ions have large energy can create electron-hole pairs in a semiconductor device [1]. The radiation effects on semi conductors are mainly classifies as follows

A. Total Ionization Dose effects

Total ionization dose (TID) effects on active devices are a long term exposure of electronic components to radiation. The total amount of ionization dose depends on radiation intensity and amount. These effects cause some major impacts on semiconductor devices i.e threshold Voltage Variation due to holes trapped in SiO2 and threshold Voltage Variation due to Si/SiO2 surface change [2].

B. Single Event Effects

Single Event Effects (SEEs) are caused by a single energetic particle and can take on many forms striking out a semiconductor device. The particle transfers the energy to the device material when it transverses through the device. Single Event Upsets (SEUs) are soft errors, and non-destructive. They normally appear as transient pulses in logic or support circuitry or as bit flips in memory cells or registers. Several types of hard errors, potentially destructive can appear. Single Event Latch up (SEL) results in a high operating current above device specifications and must be cleared by a power reset. Other hard errors include Burnout of power MOSFETS, Gate Rupture, frozen bits, and noise in CCDs [1], [2].

Single event phenomena can be classified into three effects (in order of permanency):

a) Single event upset (soft error)

b) Single event latch up (soft or hard error)

c) Single event burnout (hard failure)

C. *Other Radiation Effects*

Besides threshold voltage variation and the single event effects, radiation effects also include the larger sub-threshold current, the larger leakage current and the degraded mobility. Different circuits may have different performance degradation under radiation. Normally digital circuits are more sensitive to the single event effect which may upset the logic state. On the other hand the performance of the analog circuit may easily be affected by the threshold voltage variation [1]-[3].

All these effects cause some major impacts on CMOS devices, such as the switch point, the decreased output rail voltage, and the increased leakage current. If radiation becomes instance enough proper inverter operation fails. We propose a scheme to maintain the output voltage by making V_{gs} negative when the NMOS cuts off [4].

This paper shows the structural CMOS with and without radiation and variation of electrical properties of device under various radiations doses and proposes a modified CMOS structure that mitigates radiation effect by improving switch point in I-V characteristic.

To redesign the circuit for radiation resistance; the radiation hardened inverter circuit is implemented in each stage of Voltage Controlled Oscillator (VCO) design [4], [5].

II. SIMULATION DETAILS

Radiation dose is defined as the amount of energy deposited into unit mass of the material of interest. The units of radiation dose are 1 Gy (Gray) = 1 Joule/Kg = 100 rads. Since this energy loss is material dependent, the type of the material is appended onto the unit. A dose is always

referenced to a mass of material. The term dose rate is used to indicate the dose per unit time (e.g. Gy/min or Rad/min) that a device will experience at a position from a radiation source.

Devices simulation is split into two distinct models that are calculated simultaneously at each DC bias point or transient time step.

l. Optical ray trace using real component of refractive index to calculate the optical intensity at each grid point.

2. Absorption or photo-generation model using the imaginary component of refractive index to calculate a new carrier concentration at each grid point.

Here we define the photo-generation rate in a C-INTERPRETER function written into a text file that can be supplied to the program. The file returns a time and position dependent photo-generation rate to the program. This returned value is multiplied at every node point.

The X. ORIGIN, Y. ORIGIN and X. END, Y. END parameters set the coordinates of the starting and the last point of the line segment. The default values correspond to the top left and bottom left corners of the device considered.

The Standard beam input syntax allows specification of plane waves with Gaussian or flat-top (top-hat) irradiance profiles.

In this simulation, we have assumed that the radiation on the CMOS Latch up device has created a uniform Photo-generation rate of 1×10^{25} s^{-1} cm^{-3} within the CMOS device.

III. CMOS STRUCTURES AND CHARACTERISTICS WITH AND WITHOUT RADIATION

CMOS-Bulk Devices (IC's) experience "latch up" due to a parasitic four-layer PNPN path, inherent in most unhardened devices. These parasitic four-layer devices acts like a Silicon Control Rectifier (SCR) which once latched cannot be turned off without shutting off the power.

If the CMOS-bulk process creates parasitic SCR's or PNPN structures then the excessive charge may cause a Latch up leading to a SEL which can sometimes lead to the destruction of the device.

Another potentially catastrophic SEE phenomenon called “Snapback” exhibits many of the characteristics of latch up and can occur in single MOS transistors structure [5]. A single high energy particle may trigger snapback if the field across the drain region is sufficiently high. Snapback is due to the prospect of a parasitic bipolar transistor existing between the drain and source region of a MOS transistor which amplifies avalanche current that results from the transversal of the heavy ion Cosmic ray particle. This results in a very high current between the drain and source region of the transistor with subsequent localized heating.

In the basic CMOS inverter circuit after irradiation the most important changes are the switch point, the decreased output rail voltage and the increased leakage current. If radiation becomes strong enough, proper switching operation may fail as shown in fig.5 and fig. 6 [4].

The uniform photo-generation rate of 1×10^{25} s^{-1} cm^{-3} is defined using ATLAS C-INTERPETER function as shown on the Fig. 3 and Fig. 4.

Simulator calculates optical intensity profile within the semiconductor device, and converts these profiles into photo generation rates. This unique coupling allows us to simulate electronic response to optical signals for aboard range of devices.

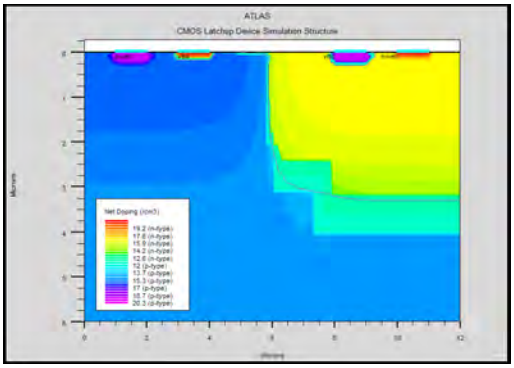

Fig. 1 CMOS Latch up device simulator structure.

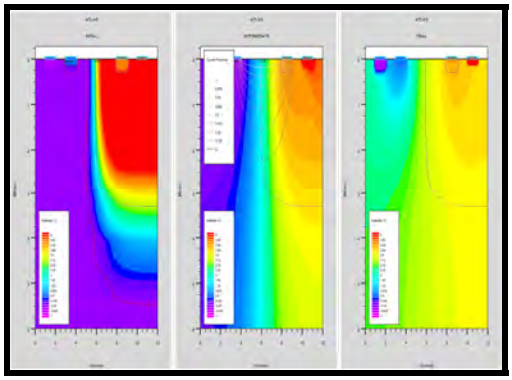

Fig. 2 Initial, Intermediate & Final Potential Contour Plots of CMOS Device without Radiation.

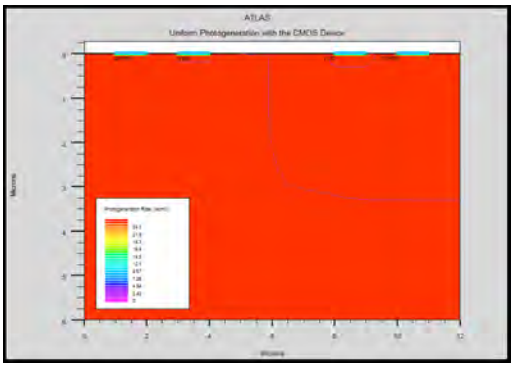

Fig. 3 Uniform photo-generation contour plot of the CMOS device.

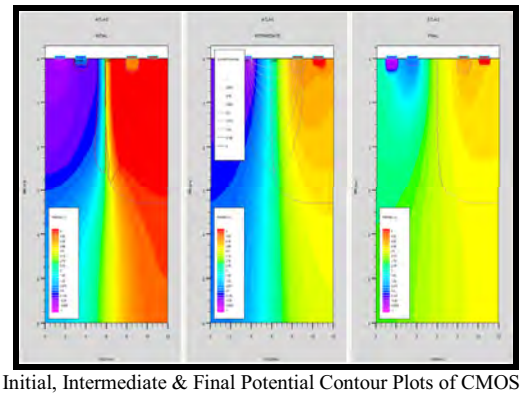

Fig. 4 Initial, Intermediate & Final Potential Contour Plots of CMOS Device with Radiation.

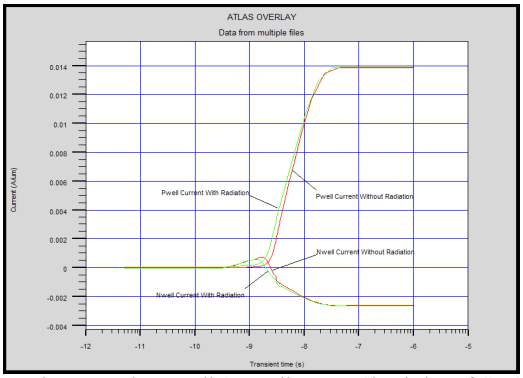

Fig. 5 Transient Pwell & Nwell current Simulation of CMOS Device with and without Radiation.

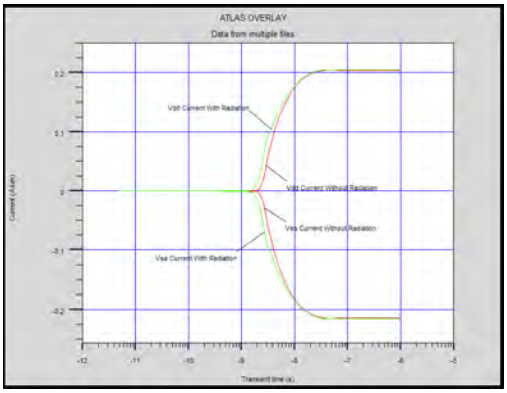

Fig. 6 Transient Vdd & Vss current Simulation of CMOS Device with and without Radiation.

IV. DESIGN OF RADIATION HARDEN VOLTAGE CONTROL OSCILLATOR (VCO)

A. Voltage Controlled Oscillator (VCO)

The VCO is a circuit which can tune the oscillator output frequency from the control voltage. The linear function of the frequency vs. voltage is shown below.

$$\omega_{out} = \omega_o + K_{VCO} V_{CTRL}$$

Where W_0 is the free running frequency and K_{VCO} is the gain of the VCO, expressed in rad/s-V. Fig. 8 shows the VCO transfer characteristic [6].

A Voltage Controlled Oscillator or VCO is an electronic Oscillator designed to be controlled in Oscillation frequency by a voltage input. One of the most important design specifications for a VCO is its frequency versus control voltage characteristic. If this characteristic changes due to radiation, it will affect the central frequency of the VCO as well as its tuning range resulting in an unstable PLL. Therefore it is desirable to have a VCO of frequency which remains unchanged at a given control voltage in the presence of radiation [4], [5], [6], [7].

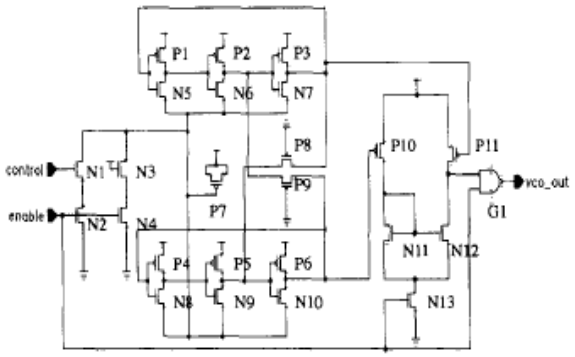

Fig. 7 Generic VCO, The synchronized ring oscillators, control device, and diff. Stage.

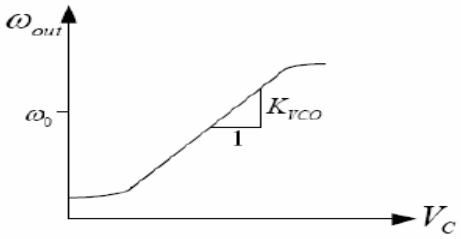

Fig. 8 VCO transfer characteristic.

Schematic diagram for Voltage Controlled Oscillator circuit showing the VCO in Fig.7 consists of two synchronized current controlled ring oscillators with an NMOS current source. A differential stage which has transistors PIO-PI 1, NI 1-Nl3, G1 and that converts the output of the cross coupled rings to single ended and restores the VCO voltage swing to full rail. This circuit topology has excellent noise rejection in the order of 1 ps/mV of power supply noise and wide bandwidth over 100 MHz even for supply voltages less than 3 V. A dedicated analog supply pin

is provided for the VCO and charge pump to minimize power supply induced clock jitter [4], [6]. The VCO is designed in a way that its gain curve falls within the range of interest for all process corners and conditions resulting in a gain of 130 MHz/V

B. Ring Oscillator Circuits

In the circuit of Ring Oscillator, The cross coupled transistors (transistors P8, P9) synchronize the two oscillators transistors Pl-P6, N5-NlO, so that they run at 180" out of phase. The devices conduct enough current to synchronize the oscillators immediately after power up as well as to keep them 180" out of to a differential stage which restores full rail-to-rail swing. An NMOS transistor is used to convert the reference voltage from the *RC* filter into pull-down current for the VCO transistor, NI. The W/L is selected to maximize the control voltage range while the length was made long to minimize short channel effects. The ground reference of NI is the same as the one of the filter capacitor which helps to ensure that the V and I_d of N1 are unaffected by ground bounce. A parallel current path is provided to ensure oscillation for low control voltages. A long channel transistor i.e. N3 connected in parallel with the control NMOS transistor named , Nl ,conducts a small amount of dc current in order to guarantee that the VCO oscillates at a minimum frequency even when the control device operates in the sub threshold region[5],[6**].**

C. Radiation Hard Voltage Controlled Oscillator

One of the most important design specifications for a VCO is its frequency versus control voltage characteristic. If this characteristic changes due to radiation, it can affect the central frequency of the VCO as well as its tuning range resulting in an unstable PLL, where VCO used. Therefore in the presence of radiation, it is desirable to have a VCO of which the frequency remains unchanged at a given a control voltage. Keep in mind above problem; we switched over to Radiation Hardened Circuit [5]-[7].

The VCO circuit is shown in Fig. 9, it includes two current-controlled ring oscillators i.e. M12-M23 and M24-M35 which is used for noise rejection. In each ring oscillator design there are three inverters and each inverter consists of four transistors for rad-hard purposes. The total current of oscillators is provided by M3 and M5-M8 and transistor M3 converts the control voltage to current while M5-M8 provides minimum current for ring oscillators when M3 is off. The sum of the current is mirrored through M10, M11 and then controls the ring oscillators. The cross coupled transistors M28, M29 synchronize the two oscillators so that the outputs are 180˚ degrees out of phase which are required. The simple diff-amp (M38-M42) converts the outputs of two ring oscillators to a single ended value and restores the VCO output voltage swing to full rail-to-rail output[4],[5].

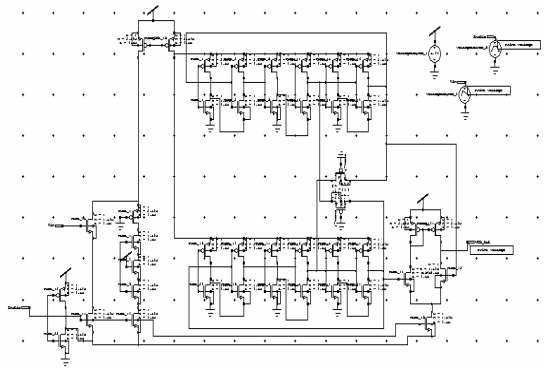

Fig. 9 Radiation Hard VCO circuit.

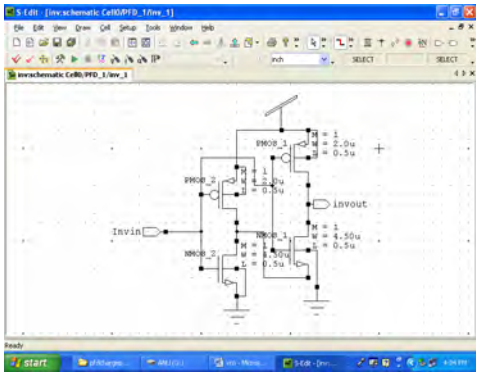

Fig.10 Design of Radiation Hard Inverter.

V. RESULTS AND DISCUSSION

This paper focuses on the simulated results for the radiation hardened CMOS inverter. The first section shows the simulation results prior to radiation and post radiation using radiation hard model file and second section shows the radiation harden by Design (RHBD) Voltage Control Oscillator (VCO).

It is shown that TID effect increased the threshold voltage of both NMOS and PMOS transistors by about 0.2 V.

Since other parameters have not yet been extracted, they cannot be adjusted in this radiation hard model file. Because V_{tho} and mobility are main parameters of MOSFETs. This post radiation simulation shows the basic degradations of inverter performance due to radiation effect. Accordingly, this simulation can help optimize our radiation hard circuit design of VCO.

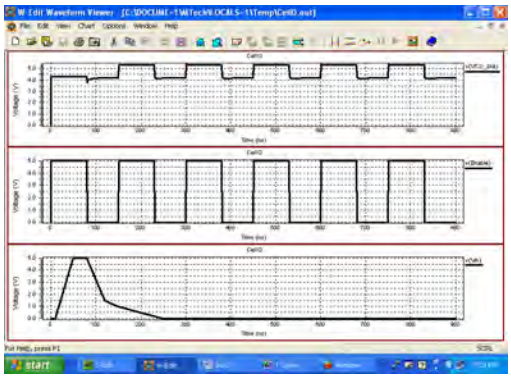

Fig. 11 VCO Output

ACKNOWLEDGEMENT

The author wishes to acknowledge Prof. A. Shastri for guiding and providing research facilities at Banasthali University. The author (CPJ) is grateful to Department of Science and Technology (DST), New Delhi for supported this work through SERC grant.

REFERENCES

[1] Allan H. Johnston, Fellow, IEEE, and B. G. Rax, "Failure Modes and Hardness Assurance for Linear Integrated Circuits in Space Applications", IEEE Transactions on Nuclear Science, Vol. 57, No. 4, August 2010.

[2] P. E. Dodd, Fellow, IEEE, M. R. Shaneyfelt, Fellow, IEEE, J. R. Schwank, Fellow, IEEE, and J. A. Felix, Member, IEEE, "Current and Future Challenges in Radiation Effects on CMOS Electronics", IEEE Transactions on Nuclear Science, Vol. 57, No. 4, August 2010.

[3] Srikanth Jagannathan, Daniel R. Herbison, William Timothy Holman, and Lloyd. W. Massengill, "Behavioral Modeling Technique for TID Degradation of Complex Analog Circuits", IEEE Transactions on Nuclear Science, Vol. 57, No. 6, December 2010.

[4] Rajat Sengupta, Student Member, IEEE, Bert Vermeire, Senior Member, IEEE, Lawrence T. Clark, Senior Member, IEEE, and Bertan Bakkaloglu, Senior Member, IEEE, "A 133 MHz Radiation-Hardened Delay-Locked Loop", IEEE Transactions on Nuclear Science, Vol. 57, No. 6, December 2010.

[5] Vincent Von Kanel, denial Aebiscber, Christain and Evert Dijkstra," A 320 MHz 1.5 MW @ 1.35V CMOS PLL for Microprocessor Clock generator," IEEE Journal Solid-State Circuit, Vol.31 no.11, Nov 1996, pp1755-1722

[6] Jer-Fu Dennis Wu, "Phase locked loop for radiation hardened Environment", The University of Texas at Arlington, Dec. 2006

[7] Ethan H. Cannon and Manuel Cabanas-Holmen, Member, IEEE", Heavy Ion and High Energy Proton-Induced Single Event Transients in 90 nm Inverter, NAND and NOR Gates", IEEE Transactions on Nuclear Science, Vol. 56, No. 6, December 2009."