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A 180 nm Low Power CMOS Operational Amplifier

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***Abstract*—This paper presents the design of two-stage operational amplifier (Op Amp). The circuit was designed in standard 180 nm digital n-well CMOS process. The design consists of very less number of transistors, hence the design is area optimized. Achieved open loop gain of the amplifier is 74.89 dB. The unity gain bandwidth (UGB) is 7.3 MHz and the phase margin is 48 degree with a 10 pF capacitive and 1 M ohm resistive load. The average power consumption of the amplifier is 0.402 mW and slew rate is 10 V/us.**

***Keywords*—CMOS Op Amp, Low Power, Moderate Speed**

I. Introduction

Operational amplifier is most versatile and fundamental building block in analog signal processing applications. The operational amplifier (Op Amp) is a high gain, DC coupled voltage amplifier with a differential input and, single or differential output to be used with negative feedback to precisely define a closed loop transfer function. The basic requirements for an op amp are sufficiently large open loop gain, large unity gain bandwidth, high input impedance, low output impedance, and high speed. These amplifiers are key elements of most of the analog subsystems, particularly in switched capacitor filters. For last few decades a CMOS implementation of analog circuits proved better than its counterparts as the same technology can be used to implement analog as well as digital building blocks on the same chip.

This paper is focused on the design of two-stage unbuffered operational amplifier for use within single chip mixed-signal system. In section II, the design methodology for two-stage CMOS op amp is addressed. In section III, achieved simulation results are presented. Finally, the outcomes of the design are concluded in section IV.

II. Design of Two-Stage Operational Amplifier

Currently, the most widely used circuit topology for the implementation of CMOS operational amplifier is the two-stage topology. This topology provides good output voltage swing, common mode range, open loop voltage gain, and CMRR. Circuit variations of the basic two-stage amplifier like cascode or folded-cascode topologies can also be used to improve voltage gain further but at the expense of reduced output voltage swing. For a better stability in closed loop applications, frequency compensation is necessary in operational amplifiers. A number of frequency compensation techniques are proposed to stabilize a closed loop two-stage amplifier [1]–[4]. In order to achieve good stability, other performance parameters are usually compromised. As a result good compensation technique and design methodology is needed to design an op amp that meets all specifications.

Generic block diagram of simple two-stage op amp is shown in figure 1 below. First stage consists of high-gain differential amplifier. Mostly cascading is used to enhance the gain in this stage. This stage has the most dominant pole of the system. A common source single stage amplifier is usually used as a second stage, which gives high output voltage swing. Third stage is most commonly implemented as the unity-gain source follower circuit [5].

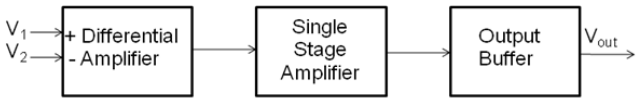

Fig. 1. Block diagram of basic op amp [5]

A. Topology Selection

For high speed and high accuracy circuits, op amps with high open-loop DC gain, large output voltage swing, and high unity-gain bandwidth are required. Our target is to design an amplifier with 5 MHz unity-gain bandwidth, and a DC gain higher than 73 dB, with a 10 pF load. Topology that will surely satisfy this magnitude of DC gain is two-stage topology. Hence two-stage topology is chosen.

B. Design Specifications

The desired specifications of the design are given in the Table I below.

TABLE I. Desired specifications of the design

Specifications	Desired value
DC open-loop gain	$\geq$ 73 dB
Unity gain bandwidth	5 MHz
Phase margin	$\geq 60°$
CMRR	$\geq$ 80 dB
Output voltage swing	$\geq$ 3 V (peak to peak)
Power dissipation	$\leq$ 1 mW
Slew rate	$\geq$ 10 V/μs
Load capacitance	10 pF
Load resistance	$1 M\Omega$
Supply voltage	$\pm$1.8 V

C. Circuit Analysis and Implementation

The first stage of two-stage op amp is input differential amplifier. Here in this design we used NMOS input pair with

current mirror load. NMOS transistors have higher transconductance compared to PMOS transistors; hence NMOS transistors were used as an input pair. For output stage a common source amplifiers has been used, which is able to provide a large gain in output stage. The advantage of common source amplifier is high output voltage swing [1]. A complete schematic of op amp is shown in figure 2.

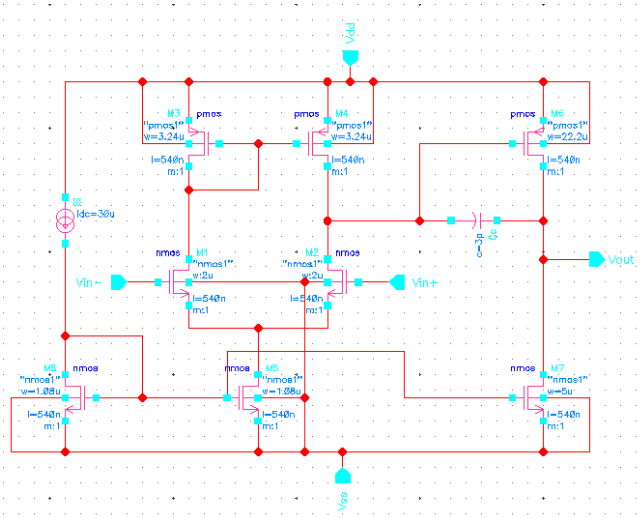

Fig. 2. Schematic of two-stage op amp

All transistors should operate in saturation region. Value of compensation capacitor is computed based on load capacitance and unity gain bandwidth requirement for 45° phase margin. Next, the minimum value of tail current I_5 is determined based upon slew rate requirement.

In first stage, M1 and M2 are input NMOS transistors, whose transconductance has a large impact on the open loop gain of the op amp. Required transconductance (g_{m1}/g_{m2}) of the input transistors is determined from the knowledge of compensation capacitance and unity gain bandwidth. Next, the size of M1 and M2 is directly computed from g_{m1}/g_{m2}. The PMOS transistors M3 and M4 should have a high output resistance so that we should get high gain. The size of M3 and M4 is determined by using the requirement for positive input common mode range. Using the negative ICMR equation, overdrive voltage of M5 is calculated, which leads to computation of size of M5.

For common source amplifier (second stage) design, the transconductance of M6 is first computed based upon loading pole and unity gain bandwidth knowledge. The size of M6 is calculated from size of M3, g_{m3}, and g_{m6}. I_6 can be calculated from the consideration of the "proper mirroring" of first-stage current mirror load. I_6 will most likely determine the majority of the power dissipation. The device size of M7 can be determined from size of M5, I_6, and I_5. Thus the total amplifier open loop gain is

$$A_v = \frac{2\,(g_{m2})\,(g_{m6})}{I_5\,(\lambda_2+\lambda_3)\,I_6\,(\lambda_6+\lambda_7)} \tag{1}$$

and total power dissipation is

$$P_{diss} = (I_5 + I_6)\,(V_{DD} + |V_{SS}|) \tag{2}$$

III. Simulation Results

To verify the correctness of the design, several simulations were performed in 180 nm CMOS technology using BSIM3v3 Spectre models.

A. Open-loop Configuration Results

A testbench to simulate op amp in open-loop configuration is shown in figure 3.

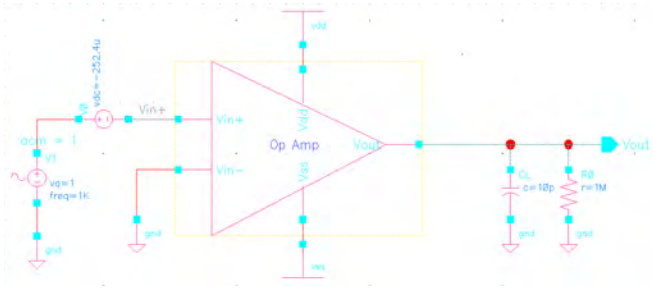

Fig. 3. Open-loop configuration testbench

Figure 4 shows the frequency response of op amp. The result shows small-signal voltage gain which is 74.89 dB and phase margin of 48° which is less than desired value. It can also be seen that the unity gain bandwidth (UGB) of op amp is 7.26 MHz.

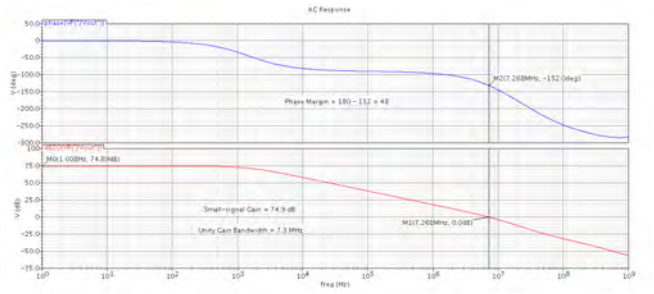

Fig. 4. Magnitude and Phase plot of op amp

B. Common-Mode Configuration Results

A testbench to simulate op amp in common-mode configuration is shown in figure 5.

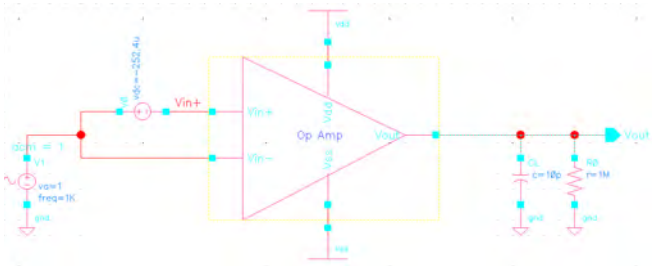

Fig. 5. Common-Mode configuration testbench

The magnitude plots for differential-mode and common-mode inputs are shown in figure 6 below. From these plots the measured CMRR is 82 dB. This implies that op amp has a better rejection to the common-mode noise.

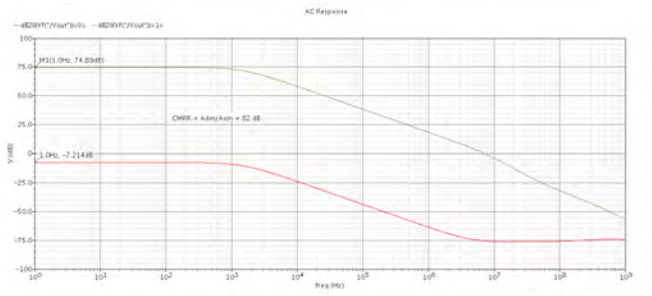

Fig. 6. Differential-mode and common-mode magnitude plot to measure CMRR

The simulation result to measure average power dissipation of the op amp is shown in figure 7. It can be seen that the average power dissipation is 0.402 mW.

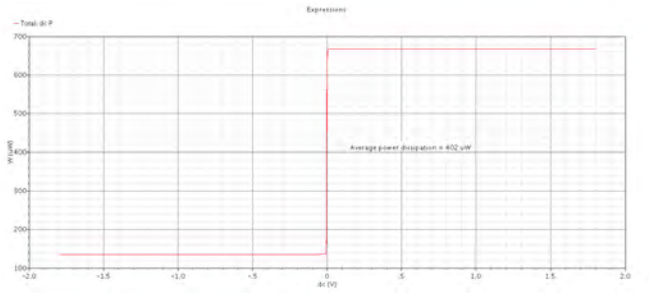

Fig. 7. Power dissipation plot of the op amp

C. Unity Gain Configuration Results

A testbench to operate op amp in unity gain mode is shown in figure 8.

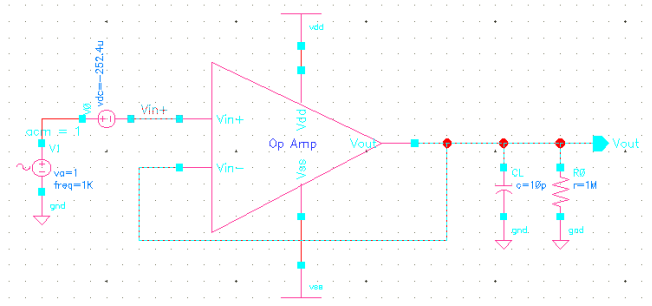

Fig. 8. Unity gain configuration testbench

Figure 9 shows the transient response of op amp in unity gain configuration. One can observe from plot that output is exactly following the input.

Figure 10 shows the plot to measure positive slew rate. From the plot it can be seen that positive slew rate is 10.2 $V/\mu s$, which satisfies the targeted value.

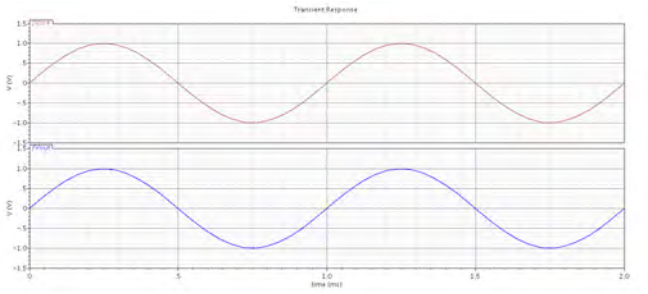

Fig. 9. Transient response of op amp in unity gain configuration

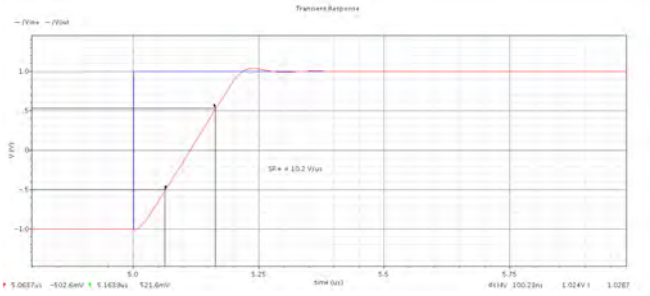

Fig. 10. Positive Slew Rate simulation result

Figure 11 shows the negative slew rate measurement plot. From the plot it can be seen that negative slew rate is 9.3 $V/\mu s$.

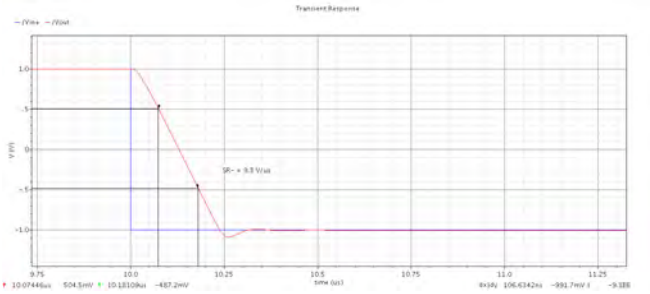

Fig. 11. Negative Slew Rate simulation result

A plot showing output voltage swing of the op amp is shown in figure 12. It can be observed that output voltage swing is from -1.7 V to +1.7 V.

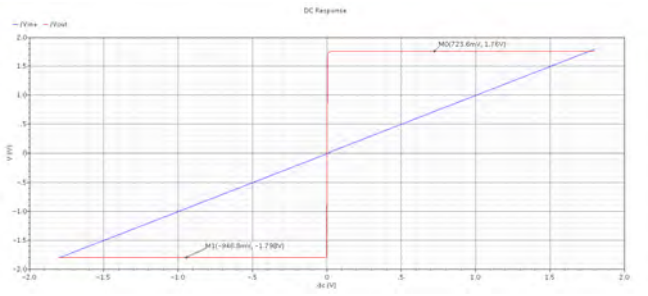

Fig. 12. Output voltage swing of op amp

Table II below shows the results which has been obtained after simulation. The discrepancies in desired values and obtained values are very less.

TABLE II. SUMMARY OF SIMULATION RESULTS

Specifications	Desired value	Obtained value
DC open-loop gain	$\geq$ 73 dB	74.89 dB
Unity gain bandwidth	5 MHz	7.26 MHz
Phase margin	$\geq 60^\circ$	48°
CMRR	$\geq$ 80 dB	82 dB
Output voltage swing	$\geq$ 3 V (peak to peak)	3.4 V (peak to peak)
Power dissipation	$\leq$ 1 mW	0.402 mW
Slew rate	$\geq$ 10 V/μs	10.2 V/μs
Load capacitance	10 pF	10 pF
Load resistance	$1M\Omega$	$1M\Omega$
Supply voltage	$\pm$1.8 V	$\pm$1.8 V

IV. CONCLUSION

Design of op amp is multidimensional optimization problem where optimization of some parameters degrades other parameters. Simulation results confirm that all targeted specifications are achieved except for the phase margin. We can achieve higher phase margin by increasing the compensation capacitance but it leads to the larger area and more dynamic power dissipation.

Here the improvement in power consumption is achieved by keeping lower tail current which also improves the DC gain of the amplifier. The design achieves slew rate of 10 $V/\mu s$. Thus it can be considered as a moderate speed op amp.

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