

Bandwidth Extension of Voltage Follower using DTMOS transistor

Shelly Garg, Geetika Chaudhary, Vandana Niranjana and Ashwani Kumar
Department of Electronics and Communication Engineering
Indira Gandhi Delhi Technical University for Women, New Delhi, India
Vandana7379@gmail.com

Abstract—In this paper, we have proposed a new approach to improve the bandwidth of unity gain voltage follower. This approach is based on using a dynamic threshold MOS transistor (DTMOS). The bandwidth of the proposed voltage follower has been enhanced by a factor of nearly 2.5. Use of DTMOS transistor also improves the input signal range of the proposed voltage follower. The proposed and conventional circuits have been mapped on to the 180nm CMOS technology. Simulations at low supply voltage of 1Volt validate the proposed voltage follower cell. A squarer circuit designed using proposed follower also shows wideband operation as compared to its conventional version. Thus proposed voltage follower is promising for low voltage wideband applications.

IndexTerms—Dynamic threshold MOS Transistor, voltage follower, low voltage, analog integrated circuits, bandwidth.

I. INTRODUCTION

Due to the tremendous downscaling of CMOS technology, the circuits working on high supply voltage are getting obsolete. In the last decade, great attention has been focused on low-power microelectronics due to the rapid development of laptops, portable systems, and cellular networks. Low power consumption has become a major consideration in circuit design [1]. The main issue with low voltage operation is that the circuit performance degrades significantly. Thus new techniques are being developed which can be incorporated in circuits to enable low voltage operation with high performance. Hence, relevant modifications in the conventional circuits are required to meet the application specific requirements [2].

Voltage buffer/follower is a basic building block for a large number of integrated circuits like analog filters, current mirrors etc. This circuit is able to sink a very large current from load but the biasing current limits its sourcing capability. Also, the small and large signal gain is limited to a value less than unity for resistive loads. Both of these setbacks are overcome by flipped voltage follower (FVF) proposed in [3] but it has a restricted range of operation and its sourcing

capability is limited by the bias current. Therefore, a better structure which overcomes the problem of operating range of FVF, called level shifted flipped voltage follower (LSFVF) is preferred [4]. In this configuration, the input and output resistance of voltage follower remains unaffected but the operating range gets enhanced. LSFVF is an upcoming low voltage technique used for designing high performance low voltage circuits. LSFVF structure seems to be a promising structure for wideband applications also.

The dynamic threshold MOS transistor (DTMOS), proposed in [5], is very suitable to be employed in circuits to be used in ultra low voltage environment. In DTMOS, body terminal is tied to the gate terminal making threshold voltage of MOS transistor (V_T), a function of the gate input. There is an increasing interest in the suitability of DTMOS for analog applications [6,7]. DTMOS transistor is implemented in triple well technology so that PMOS and NMOS bodies can be independently biased. In this work we have proposed to use DTMOS transistor to improve the bandwidth of LSFVF. The paper has been arranged as follows: In section II, conventional LSFVF and its operating range has been discussed. Section III describes the operation of the proposed LSFVF. In section IV, a squarer circuit is designed as an application of the proposed LSFVF. Simulation results are given in section V and conclusions have been drawn in section VI.

II. CONVENTIONAL LEVEL SHIFTED FLIPPED VOLTAGE FOLLOWER

The conventional LSFVF employs a DC level shifter in feedback path of M2 as shown in the Fig.1. Also, its swing is increased as compared to FVF by employing a voltage follower M3 and a current source as the DC level shifter as mentioned above. This improvement in the operating range is

dependent on the biasing current and the value of threshold voltage of transistor M3 .

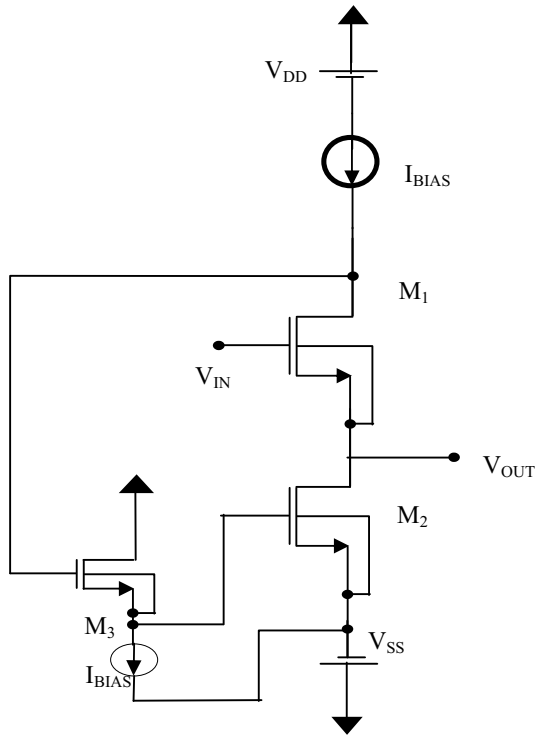


Fig.1. Conventional LSFVF

The input/output swing of the circuit will increase to $V_{inpp}=2V_T$. The complete valid input range can be given by [4]

$$\sqrt{\frac{2i_D}{K_N(W/L)_{M1}}} + \sqrt{\frac{2i_D}{K_N(W/L)_{M2}}} + V_{T(M1)} \leq |V_{SS}| + v_{in} \leq V_{T(M1)} + V_{T(M2)} + V_{T(M3)} + \sqrt{\frac{2i_D}{K_N(W/L)_{M2}}} + \sqrt{\frac{2i_{Bias}}{K_N(W/L)_{M3}}} \quad (1)$$

where V_T is threshold voltage, (W/L) is aspect ratio and i_D is drain current of MOS transistor. As seen from (1), although LSFVF has wide range but the main drawback is its poor bandwidth [8]. Hence in this work, possibility has been explored to increase the bandwidth of this circuit by employing DTMOS transistor and at the same time to maintain low voltage and low power operation.

III. PROPOSED LEVEL SHIFTED FLIPPED VOLTAGE FOLLOWER

If we connect the body terminal of MOS transistor to its gate terminal then this structure is known dynamic threshold MOS (DTMOS) transistor shown in Fig.2. In a DTMOS transistor, due to gate and body terminals shorted together, its total transconductance is enhanced from g_m to (g_m+g_{mb}) , where g_m is gate transconductance and g_{mb} is body transconductance. Thus a DTMOS transistor has higher transconductance efficiency (g_{mT}/I_D) as compared to similar MOS transistor.

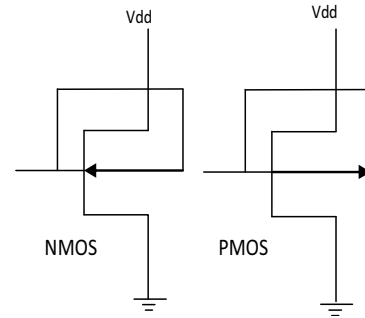


Fig.2. DTMOS transistor

In DTMOS, as gate input increases, body-source junction is slightly forward biased because of which threshold voltage drops. The threshold voltage of a MOS transistor is given as [9]

$$V_{T0} = 2\phi_B + V_{FB} + \frac{\sqrt{2q_s N_a (2\phi_B)}}{C_{ox}} \quad (2)$$

Where V_{FB} is the flat band voltage and $2\phi_B$ is the inversion layer voltage the inversion layer potential, N_a is the channel doping, ϵ_s is the Si permittivity, q is the electron charge. Considering body biasing, V_T is given by

$$V_T = V_{T0} - \lambda(\sqrt{2\phi_B} - \sqrt{2\phi_B - V_{BS}}) \quad (3)$$

Where $\lambda = \frac{\sqrt{2\phi_B N_a}}{C_{ox}}$. DTMOS operates when $V_{BS}=V_{GS}$ and as V_{BS} increases, V_T decreases. Also because of decrease in the threshold voltage, the transconductance increases. At low drain current, DTMOS shows significantly higher cutoff frequency and maximum frequency oscillator performance [10]. The source-body capacitance extends the bandwidth but

flattens the power gain. The better linearity at low drain current suggests that DTMOS transistor is an attractive option for RF applications. The circuit implementation of proposed LSFVF is shown in Fig.3. Transistors M1, M2 and M3 have been configured as DTMOS. Since power supply reduction below three times the threshold voltage will degrade circuit speed significantly, scaling of power supply should be accompanied by threshold reduction

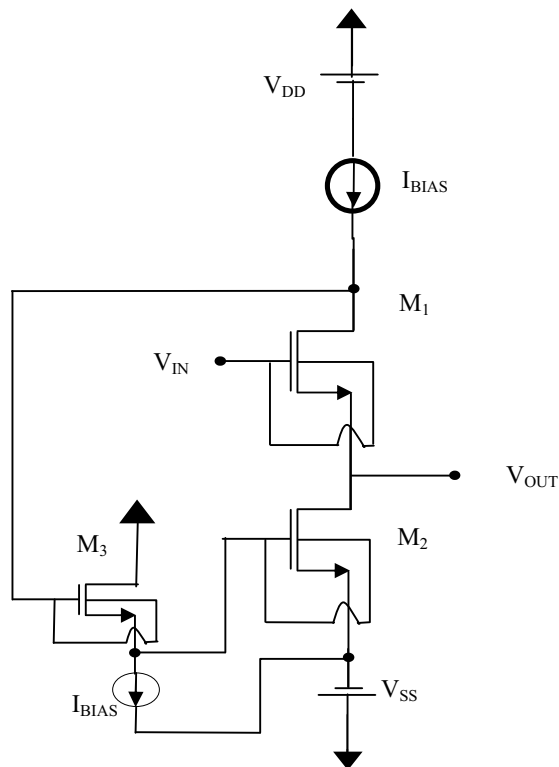


Fig.3. Proposed LSFVF

IV APPLICATION OF PROPOSED LSFVF

The squarer circuit is a basic arithmetic building block. The squarer circuit also finds its application in the design of some non linear analog circuits. For instance frequency translation, neural networks, waveform generation, four quadrant multiplier etc. [11]

In this paper, proposed LSFVF has been employed in the squarer circuit as shown in Fig.4. The proposed LSFVF is utilized with the aim of enabling low voltage operation with

high bandwidth. The proposed squarer circuit would be able to meet the increasing demands of high speed and low supply voltage applications.

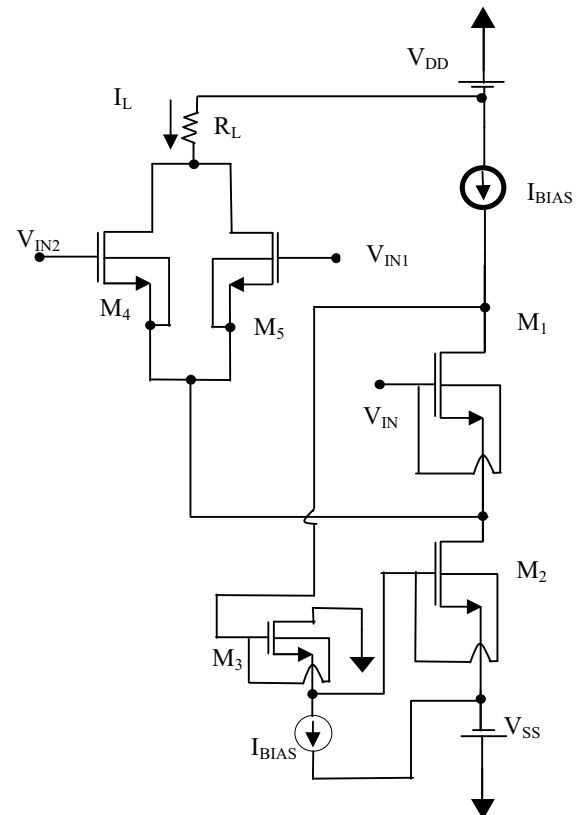


Fig.4. Squarer Circuit employing proposed LSFVF

V.SIMULATION RESULTS

The conventional and proposed LSFVF have been simulated at 1V supply voltage ($V_{dd}=0.6V$ and $V_{ss}=-0.4V$) in 180nm CMOS TSMC of MOSIS. The transistor sizes are summarized in Table.1. Fig.5 shows simulated frequency response of conventional LSFVF. Its simulated bandwidth is obtained as 2.016 GHz. The frequency response of proposed LSFVF is shown in Fig.6. Its enhanced simulated bandwidth is 5.107 GHz. Thus using DTMOS transistor, the frequency of LSFVF has been enhanced by a factor of nearly 2.5. The DC characteristics of conventional and proposed LSFVF are shown in Figs.7 & 8 respectively. The proposed LSFVF shows linearity for an input range of 0 to 1.8V in contrast to the conventional circuit which works linearly for 0 to 0.9V.

Comparison of conventional and proposed LSFVF is given in Table.2.

Frequency response of the squarer circuit employing the conventional and proposed LSFVF is shown in Figs.9&10 respectively. Table.3 shows comparison of simulated squarer circuits. It can be observed that bandwidth of squarer circuit increases by a factor of nearly 2.3 using proposed LSFVF.

Table.1 Transistor Dimensions

Transistor	W (um)	L (um)
M ₁	2.5	.5
M ₂ - M ₃	.5	.5
M ₄ - M ₅	.36	.18

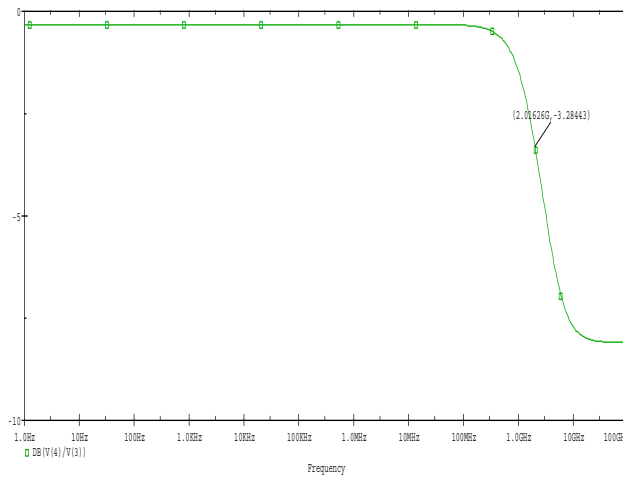


Fig.5. Frequency response of conventional LSFVF

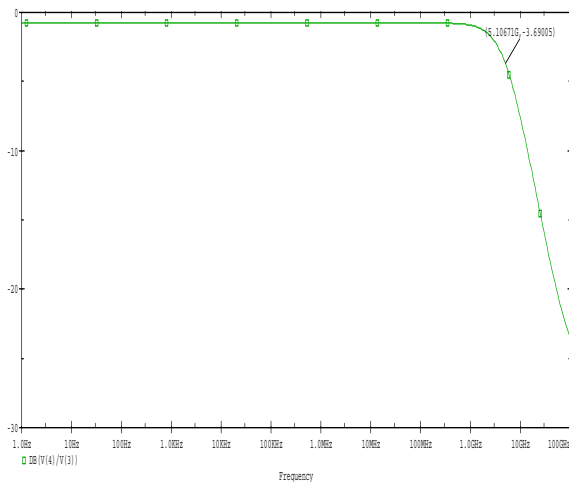


Fig.6. Frequency response of proposed LSFVF

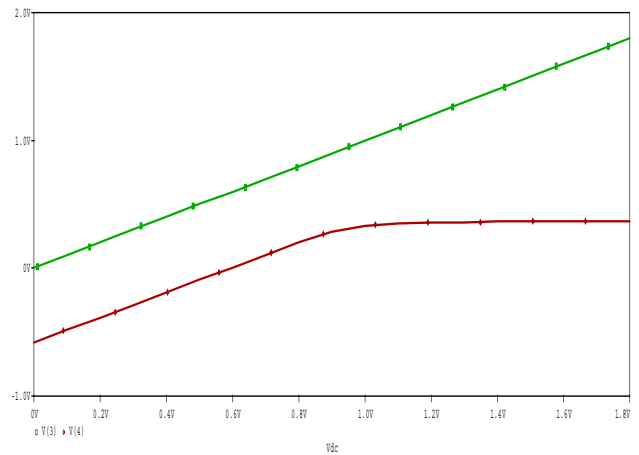


Fig. 7. DC characteristics of conventional LSFVF

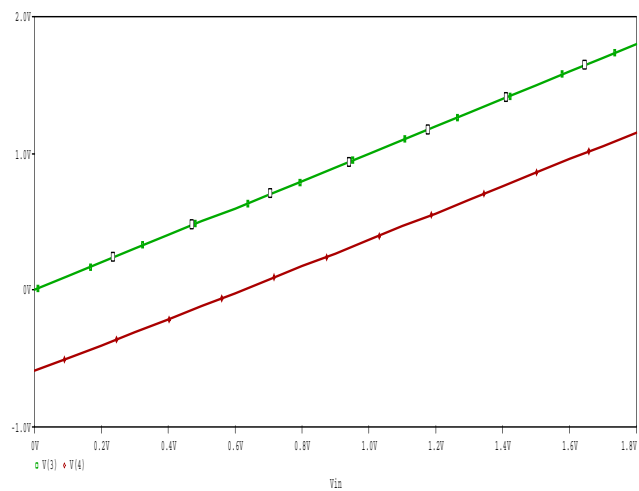


Fig.8. DC characteristics of proposed LSFVF

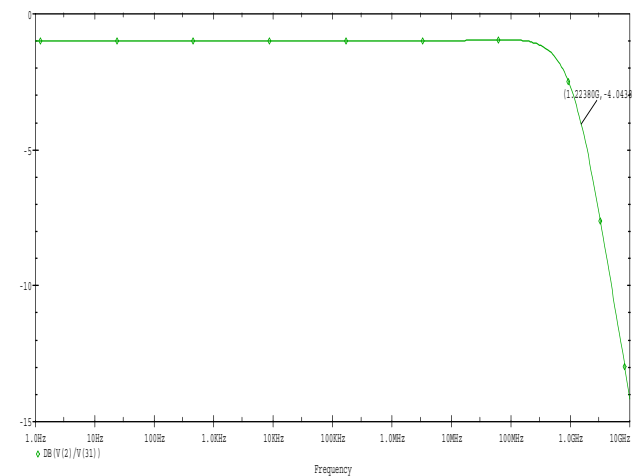


Fig.9. Frequency response of conventional squarer

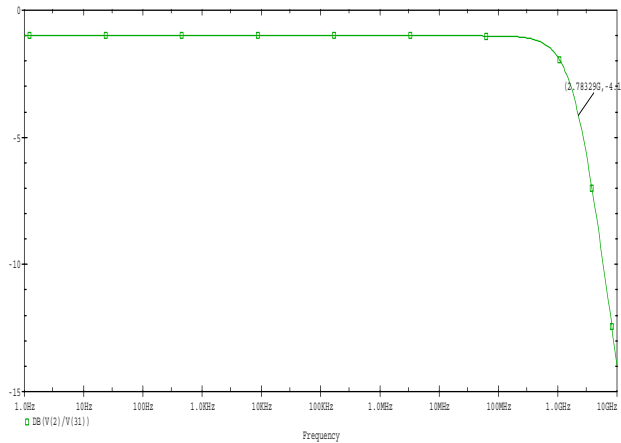


Fig.10. Frequency response of proposed squarer

Table.2. Comparison of proposed and conventional LSFVF

Parameter	Conventional LSFVF	Proposed LSFVF
Supply Voltage	1V	1V
Technology	180nm	180nm
Bandwidth	2.016 GHz	5.107 GHz
Input voltage Linear Range	.95 V	1.8 V

Table.3. Comparison of proposed and conventional squarer circuit

Simulated Circuit		Bandwidth
Squarer Circuit	Conventional	1.223GHz
	Proposed	2.783GHz

VI. CONCLUSION

In this paper we have proposed a new approach to increase the bandwidth of level shifted flipped voltage follower using dynamic threshold MOS transistor. The bandwidth of proposed voltage follower increases by a factor of 2.5. The proposed structure utilizes the advantages of dynamic threshold MOS structure to increase its bandwidth and operates at a

substantially low voltage. The input voltage range has also been increased. A squarer circuit designed using the proposed follower also shows the validity of the proposed approach of bandwidth extension. The bandwidth of squarer circuit improves by factor of nearly 2.3. Thus proposed voltage follower seems promising for wideband low voltage applications.

REFERENCES

- [1] Rajput, S.S. &Jamuar, S.S., "Low Voltage analog circuit design techniques", IEEE Circuits and Systems Magazine, Vol.2, No.1, pp.24-42, 2004.
- [2] Fabian Khateb, Salma Bay Abo Dabbous, Spyridon Vlassisa, "Survey of Non-conventional Techniques for Low-voltage Low-power Analog Circuit Design", Radioengineering, Vol. 22, No. 2, 2013.
- [3] J. Ramirez-Angulo, R.G. Carvajal and A. Torralba, "Low supply voltage high-performance CMOS current mirror with low input and output voltage requirements," IEEE Trans. Circuits and Systems II: Express Briefs, vol. 51, pp. 124-129, Mar. 2004.
- [4] Aggarwal, B., Gupta, M., Gupta, A.K., "A low voltage wide swing level shifted VVF based current mirror," International Conference on Advances in Computing, Communications and Informatics, pp.880-885, 2013.
- [5] Assaderaghi Fariborz et.al., "Dynamic threshold voltage MOSFET (DTMOS) for ultra low voltage VLSI", IEEE Trans. on Electronic devices, Vol. 44, No.3, pp.414-417, 1997.
- [6] Niranjana, V. et.al, "Composite transistor cell using dynamic body bias for high gain and low-voltage applications", Journal of Circuits, Systems, and Computers (JCSC), Vol. 23, No.8, 2014.
- [7] Niranjana, V. et.al., "Maximum bandwidth enhancement of current mirror using series-resistor and dynamic body bias technique", Radioengineering, Vol.23, No.3, pp. 922-930, 2014
- [8] J.Ramirez-Angulo, SheetalGupta Ivan Padilla, R.G.Carvajal, A.Torralba , M.Jime'nez , F. Munoz,andA.J.Lopez Martin, "Comparison of Conventional and New Flipped Voltage Structures With Increased Input/Output Signal Swing & Current Sourcing/Sinking Capabilities",IEEE,48th Midwest Symposium on Circuits and Systems,vol 2,pp.1151-1154,2005.
- [9] Niranjana, V. et. al., "Dynamic Threshold MOS transistor for Low Voltage Analog Circuits", International Conference on Recent Trends & Issues in Engineering and Technology, July,19-20,2014
- [10] Chun-Yen Chang et al., "Investigations of bulk dynamic threshold-voltage MOSFET with 65 GHz "normal mode" f_t and 220 GHz "over-drive mode" f_t for RF applications," Symposium on VLSI Technology,pp.89–90, 2001.
- [11] B. Boonchu and W. Surakamponorn, "Voltage-Mode CMOS Squarer/Multiplier Circuit" 2002 International Technical Conference On Circuits/ Systems, Computers and Communications, pp.646-649, 2002.